NEW DATA UPDATE 8

NATIONAL SEMICONDUCTOR CORPORATION

FEBRUARY 1983

NEW DATA UPDATE 8

NATIONAL SEMICONDUCTOR CORPORATION

The New Data Update 8 is provided by National Semiconductor in order to keep you abreast of the latest products available. This special issue features the first pages of data sheets published October 1982 through January 1983 (1 quarter). Two alphanumerical indexes, one by device number and one by device function, serve as guides to the contents of this Update. These indexes/tables of contents are located in the front of the book. One additional index serves as an ordering guide for all other application notes and briefs which are still available (this index is located in the back of the book).

Circle the appropriate update number on the business reply card (centerfold), add postage, and drop it in the mail to receive the complete data sheet of your choice. To order publications without an update number, please use the order number provided in the index and write it in one of the blanks provided on the reply card. Due to the costs of handling and mailing, we ask that you limit your requests to no more than 5 items.

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Please note the special discount coupons, for databooks, in the centerfold of the book.

As integrated circuits become more and more complex, the benefit of consistently high quality products becomes increasingly more important to customers, many of whom have long recognized National as *the* outstanding supplier of top quality products. Such recognition is the result of a management-driven Quality Improvement Program that has pervaded every manufacturing operation, from product design through assembly and packaging at National Semiconductor Corporation. Progress has been nothing less than dramatic, and National's commitment to quality will remain unrelenting in the decades to come.

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National Semiconductor Corporation 2900 Semiconductor Drive Santa Clara, California 95051 Tel: (408) 721-5000 TWX: (908) 339-9240

National Semiconductor

November 1982

ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer

General Description

The ADC0833 series is an 8-bit successive approximation A/D converter with a serial I/O and configurable input multiplexer with 4 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, as well as with standard shift registers or μPs.

The 4-channel multiplexer is software configured for single-ended or differential inputs when channel assigned by a 4-bit serial word.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

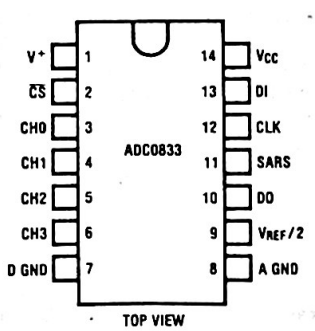
- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand alone"
- Works with 2.5V (LM336) voltage reference
- No full-scale or zero adjust required
- Differential analog voltage inputs
- 4-channel analog multiplexer
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- T^2L/MOS input/output compatible
- 0.3" standard width 14-pin DIP package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±1/2 LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	25 mW
■ Conversion Time	32 μs

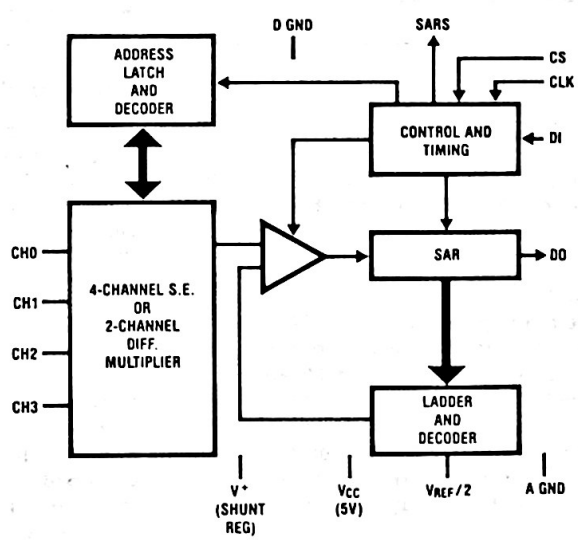
Connection Diagram

Dual-In-Line Package



TOP VIEW

Functional Diagram



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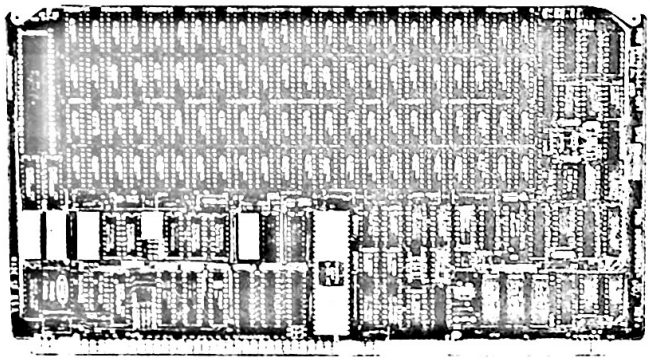
Circle DATA UPDATE No. 100595

National Semiconductor

October 1982

BLC-0512B
512K-Byte Memory Card Family



- **Features**
  - Error checking and correction
  - Selectable interrupt for uncorrectable errors
  - Selectable interrupt for single bit errors
- **Enhanced Systems Performance**
  - On-board refresh and control logic
  - Internal (transparent) refresh
  - Optional external refresh
  - Battery backup capability
- **MULTIBUS™ IEEE 796 Standard**
- **Compatible with all Series/80 Boards and Card Cages**
- **Flexible Systems Capability**
  - 8- or 16-bit data bus
  - 16-, 20- or 24-bit memory addressing
  - 8- or 16-bit I/O addressing
- **Ease of Maintenance**
  - Control status register logs failures for CPU
  - All RAMs socketed
- **One Year Warranty**

Product Overview

The BLC-0512B RAM memory cards are designed to meet the user's increasing memory requirements while maintaining a high level of data integrity. The card is available in 128, 256, 384, and 512K bytes of memory. The error correction feature enhances data integrity.

ECC is a method to detect and correct errors which may occur while reading data from the RAM. In the event a data error occurs, the CPU is notified. Error information is also logged in the Control Status Register (CSR). Selectable interrupts allow the user to determine which interrupt request line is used. Any two of eight interrupt lines may be selected. Single bit errors set one interrupt and double bit errors set a separate interrupt. Both may be assigned the same interrupt.

Functional Description

The BLC-0512B is a 512K byte (256K x 22) random access memory card designed to be compatible with all Series/80 microcomputers. Utilizing the available options, the BLC-0512B is operational in a wide variety of configurations including 8- or 16-bit I/O addressing. Set via a DIP switch, the starting address may be set on any 4K byte boundary within the 16M byte range.

Control Status Register

ECC error information is stored in an on-board CSR. The CSR is a software addressable 16-bit Control Status Register. The CSR may be set to respond to 1 of 64,536 word addresses, or if operated in the byte mode, it will respond to two consecutive byte addresses. By performing a minor jumper change, the CSR will operate with an 8- or 16-bit I/O address.

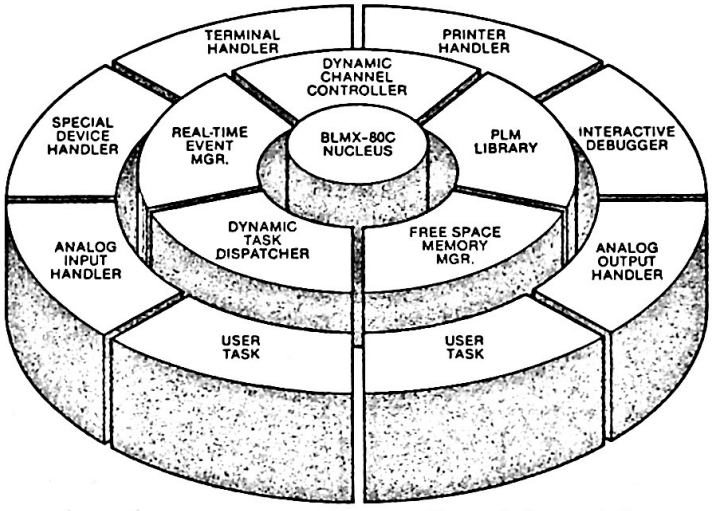
Circle DATA UPDATE No. 101527

National Semiconductor

September 1982

BLMX-80C

Board-Level, Multitasking Executive for NSC800™-Based Systems



- **Configurability**
  - Fully user configurable
  - Menu selection procedure
  - Hardware independent
- **Compatibility**
  - NSC800, Z80®
  - Bus-like structure
- **Reliability**
  - Small, efficient nucleus
  - Simple user interface
  - Standard data structures
- **User-Oriented Support**
  - Extensive I/O handlers
  - Analog handlers
  - Linkable interactive debugger
- **Easy-to-Use**
  - Prompting menus guide system configuration
  - Comprehensible system functions
  - Functional similarity for internal and external calls
  - Reconfigurable

Product Overview

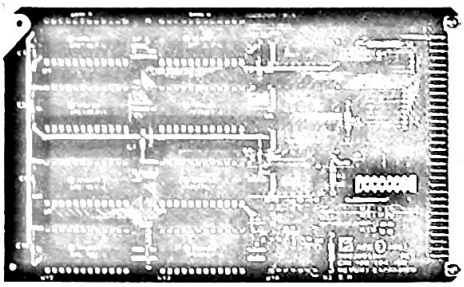
The BLMX-80C software system is a real-time, multitasking executive, specifically designed for use with National Semiconductor Corporation's CMOS Industrial Microcomputer (CIM™) products, but is equally usable for any NSC800-based system. It has been optimized for real-time applications such as process control, manufacturing monitoring, and data acquisition systems. The BLMX-80C Executive is fully modular and can readily be configured to suit applications needs. It is completely hardware and location independent, thereby providing a fundamental base upon which users can build a wide range of applications systems. In addition, BLMX-80C provides a bus-like structure that helps to integrate software with its underlying hardware through predefined data structures and interconnect procedures. This concept of software-bus architecture ensures maximum quality of standardization for compatibility and future expandability.

The BLMX-80C nucleus requires only 512 bytes of RAM and 2K bytes of ROM. The system contains all major real-time functions including task scheduling, intertask communication and synchronization, interrupt handling and I/O control, as well as many optional features.

BLMX-80C provides support for all CIM CPU boards: CIM-801, CIM-802, and CIM-804, as well as the CIM-201 Serial I/O Board and the CIM-411 and CIM-421 Analog I/O Boards. Real-time modules include a handler for the System-Level Fail-Safe Timer and cold/warm start initialization. A linkable, interactive, system-level debugger is also supplied.

Circle DATA UPDATE No. 114300

CIM™-100/104/108 Memory Expansion Boards



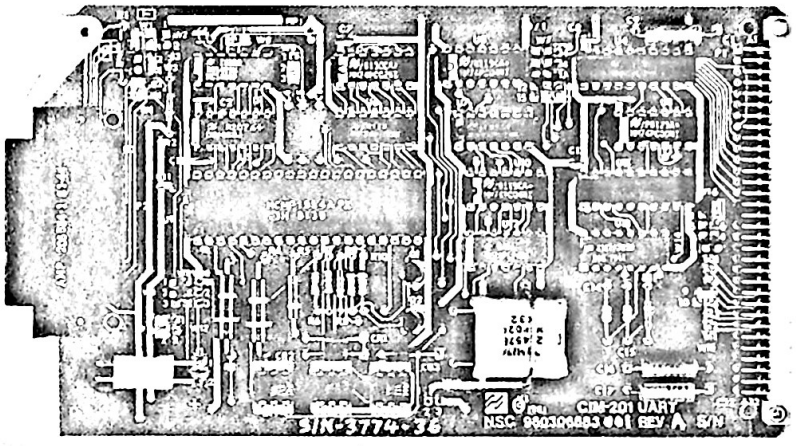
- Adds RAM and/or PROM to a SERIES/800™ system
- Supports 2k × 8 PROM/RAM and 4k × 8 PROM devices
- Address-assignable on 16k boundaries
- High performance, low power P²CMOS™ and CMOS technology
- Fits CIM-602/604 card cage
- All required connections for CIMBUS™ compatibility provided on-board
- Single 5 V_{DC} power supply
- −40°C to +85°C (−40°F to +185°F) operating temperature range
- Built solely with components burned in to A+ levels

Product Overview

The CIM-100 series of PROM/RAM Memory Expansion Boards are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-100/104/108 PROM/RAM Memory Expansion Boards are the memory expansion boards for the SERIES/800 CMOS industrial microcomputers from National Semiconductor Corporation. The CIM-100/104/108 boards are identical except for the amount of factory-installed RAM: the CIM-100 has no RAM installed, the CIM-104 has 8k RAM installed, and the CIM-108 has 16k RAM installed. The CIM-100 series boards allow various combinations of PROM and RAM to be added to a CIMBUS system, up to a maximum of 8k PROM + 8k RAM, 16k PROM, 16k RAM, or 32k PROM. The CIM-100 series memory expansion boards, only 100 mm × 160 mm (3.9″ × 6.3″) in size, fit the CIM-602/604 series card cages, and are connected to the CIMBUS by 64-pin, pin-in-socket DIN 41612 connectors. See the CIMBUS System Bus Specification Manual for a description of the CIMBUS (order as CIMBUSM or Manual #420306681-001). The use of P²CMOS and CMOS technology gives high performance at low power consumption levels, and, in keeping with the aims of the SERIES/800 line, the CIM-100 series boards are designed for reliable performance over a wide range of harsh environmental conditions.

CIM™-201 Serial Input/Output Board

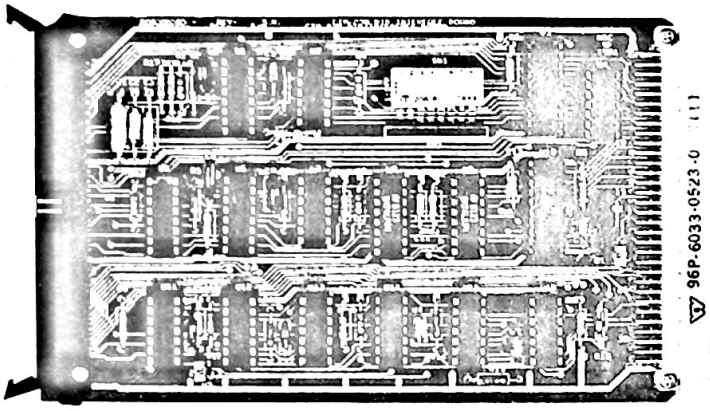


- Single-channel asynchronous transfer of serial data
- RS-232C or optically isolated 20 mA current loop operation
- Interfaces with wide variety of terminals, computers, printers, and other peripheral equipment
- May be configured as either data set (DCE) or data terminal (DTE)
- Can be used in pairs in demand/response mode
- User-selectable baud rates from 50 to 153600
- Standard 25-pin "D" connector for serial data
- CIMBUS™-compatible with SERIES/800™ line
- Small 100 mm x 160 mm Eurocard form fits directly into CIM-602/604 card cages
- P²CMOS™ and CMOS technology give high reliability at low power consumption
- −40°C to +85°C (−40°F to +185°F) operating temperature range
- Designed for demanding use under harsh environmental conditions
- Built solely with components burned in to A+ levels

Product Overview

The CIM™-201 Serial I/O Board is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS™ NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS™, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the

CIM™-230
Distributed I/O Bus (DIB™) Interface Board

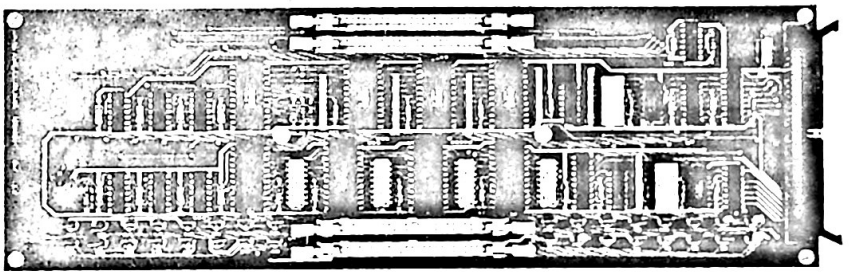


- **Provides the interface between the CIMBUS™ and the DIB**
- **Small (100 mm x 160 mm) single-wide Eurocard form fits CIM-602/604 card cages**
- **P²CMOS™ and CMOS technology give high reliability at low power consumption**
- **−40°C to +85°C (−40°F to +185°F) operating temperature range**
- **Built solely with components burned in to A+ levels**
- **DIB offers advantages for many applications**
  - —Software I/O routines are the same for all DIB I/O
  - —Single 60-pin flat cable used to interface/multi-drop up to 256 input ports and 256 output ports
  - —Polarized interface hardware ensures correct connections
  - —Switched high voltage/current interfaces remote from card cage
  - —Form factor and mounting method for user-designed DIB boards dictated only by application convenience

Product Overview

The CIM-230 Distributed I/O Bus (DIB) Interface Board is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

CIM™-311 · Power I/O DIB™ Board

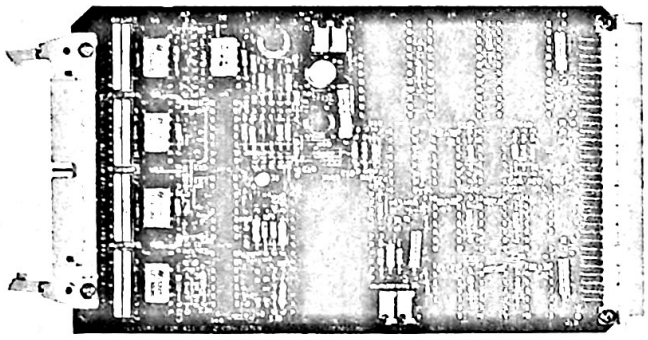


- **Allows the instant addition of popular solid state relay racks to a CIMBUS™ system**
  - Provides high voltage/current switching
  - Isolates switching-induced noise from the computer bus
  - Provides terminal strips for interface connections
- **Four maskable interrupts on positive or negative-going signals, or on any change of state**
- **Interfaces to a CIMBUS system via the Distributed I/O Bus (DIB)**
- **−40°C to +85°C (−40°F to +185°F) operating temperature range**
- **P²CMOS™ and CMOS technology provides high reliability**
- **Built solely with components burned in to A+ levels**

Product Overview

The CIM™-311 Power I/O DIB™ Board is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS™ NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS™ , a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

CIM™-411
Analog Input Board



- 32 single-ended, 16 differential, or 8 differential and 16 single-ended channels
- CPU program scan control: interrupt, hold, poll, or hold and poll
- Continuously adjustable input ranges between 1 to 2 and 10 to 20, or 4 mA to 20 mA current loop
- 12-bit resolution
- 50 μs conversion time
- P²CMOS™ and CMOS technology give high reliability at low power consumption
- −40°C to +85°C (−40°F to +185°F) operating temperature range
- CIMBUS™-compatible with SERIES/800™ line
- Small (100 mm × 160 mm) single-wide Eurocard form fits CIM-602/604 card cages
- Built solely with components burned in to A+ levels

Product Overview

The CIM-411 Analog-To-Digital Converter Board is a member of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-411 A/D board provides analog-to-digital input for a SERIES/800 system. Under program control, it will bring 12 bits of converted analog data into the system in an interrupt, hold, poll, or hold and poll mode. The CIM-411 is capable of receiving 32 single-ended inputs, 16 differential inputs, or a combination of 8 differential and 16 single-ended inputs. Conversion time is 50 μs with a full-scale input sensitivity selectable in two ranges, ±0.5V to ±0.7V or ±5.0V to ±7.0V differential, or 0.5V to 0.7V or 5.0V to 7.0V

CIM™-421
Analog Output Board

- **Two output channels**
- **12-bit resolution**
- **Voltage or current-mode outputs**
  —0V to +10V
  — −10V to +10V
  —4 mA to 20 mA current loop
- **P²CMOS™ and CMOS technology give high reliability at low power consumption**
- **−40°C to +85°C (−40°F to +185°F) operating temperature range**
- **CIMBUS™-compatible with SERIES/800™ line**
- **Small (100 mm × 160 mm) single-wide Eurocard form fits CIM-602/604 card cages**
- **Built solely with components burned in to A+ levels**

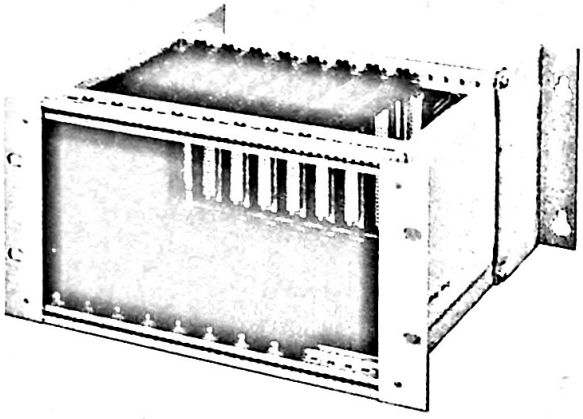
Product Overview

The CIM-421 Analog Output Board is a member of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-421 analog output board provides the capability for digital-to-analog output from a CIMBUS system. Under program control of the CIMBUS microcomputer board, it will convert 12 bits of digital data to an analog signal of 0V to +10V, −10V to +10V, or 4 mA to 20 mA on either of two available output channels. The P²CMOS and CMOS technology employed allows an operating temperature range of −40°C to +85°C (−40°F to +185°F).

The CIM-421 shares the small 100 mm × 160 mm (3.9″ × 6.3″) single-wide Eurocard form factor with the rest of the SERIES/800 line and fits the CIM-602/604 card cages. It is completely CIMBUS compatible through pin-in-socket DIN 41612 connectors, which provide an added element of mechanical and electrical reliability by eliminating the usual card-edge connector. See the CIMBUS System Bus Specification (#420206681-001) for a description of the CIMBUS. The CIM-610 voltage regulator board supplies the +5V and ±15 V_{DC} power for the D/A converter.

CIM™-602/604
CIMBUS™ Card Cages



- **Two versions**
  CIM-602: 8 slots, 10.5 inches wide
  CIM-604: 18 slots, 19 inches wide
- **Backplane and power supply connectors included**
- **Prototyping slots included in CIM-604**
- **Full access to active system components/ signals available with CIM-640 Extender Board**
- **Provisions for front or rear mounting**
- **NEMA enclosure and RETMA chassis-compatible**
- **−40°C to +85°C (−40°F to +185°F) operating temperature range**
- **CIMBUS-compatible with SERIES/800™ line**

Product Overview

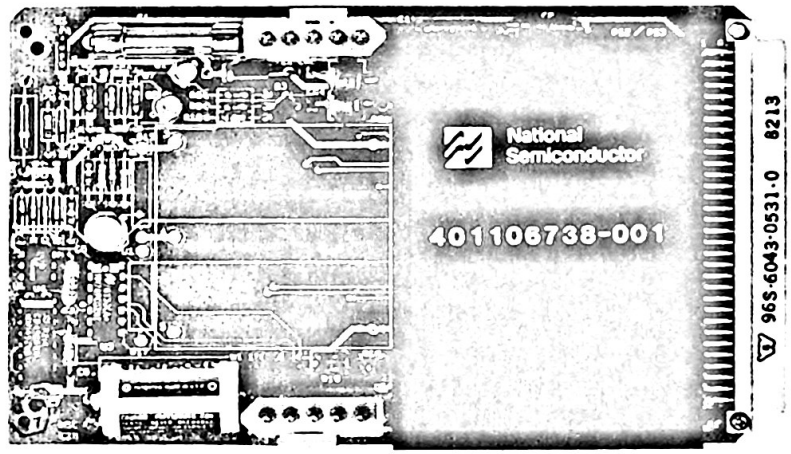
The CIM-602/604 card cages are members of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS™ NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-602/604 card cages are the standard enclosures for SERIES/800 systems. The CIM-602 is 10.5 in. (267 mm) wide and has 8 backplane slots; the CIM-604 is 19 in. (483 mm) wide and has 18 backplane slots. Both versions contain all the power and board connectors required by the CIMBUS specification, both are compatible with NEMA enclosures and RETMA cabinets, and both may be either front or rear mounted. When fully enclosed, both the CIM-602 and CIM-604 provide a rigid, durable, environment-resistant enclosure for a SERIES/800 system.

National Semiconductor

September 1982

CIM™-610 Voltage Regulator Board



- Supplies +5, +15, and −15 V_{DC} to CIMBUS™ interface
- Accepts unregulated DC input from 10.5 to 17.0 volts
- Detects both AC and DC power failures
- Provides RAM backup power from on-board lithium battery
- Self-protects against overloads, transients, and shorts
- Provides connectors for direct mounting of CIM-611 Battery Charger Board
- P²CMOS™ and CMOS technology give high reliability at low power consumption
- Operating temperatures range from −40°C to +85°C (−40°F to +185°F)
- CIMBUS-compatible with SERIES/800™ line
- Small (100mm x 160mm) single-wide Eurocard form fits CIM-602/604 card cages
- Built solely with components burned in to A+ levels

Product Overview

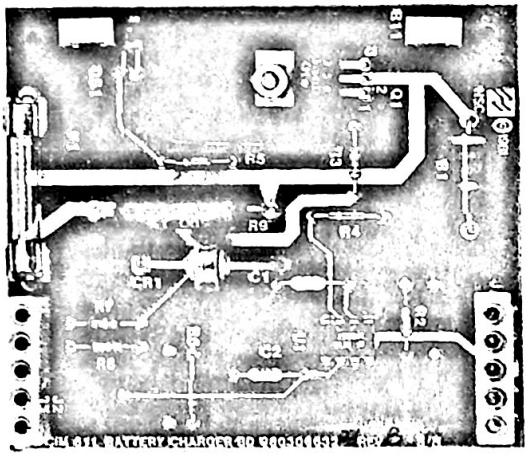
The CIM-610 Voltage Regulator Board is a member of the SERIES/800 line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-610 Voltage Regulator Board, operating on power input from either a system battery or an unregulated DC source in the range from 10.5 to 17.0

National Semiconductor

September 1982

CIM™-611 Battery Charger Board



- **Mounts directly on CIM-610 Voltage Regulator Board**
- **Automatically adjusts charge current to state of battery discharge**
- **Two charge rates — trickle and "fast"**
- **Operating temperature range from −40°C to +85°C (−40°F to +185°F)**
- **Built solely with components burned in to A+ levels**

Product Overview

The CIM-611 Battery Charger Board is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS™ NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS™, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

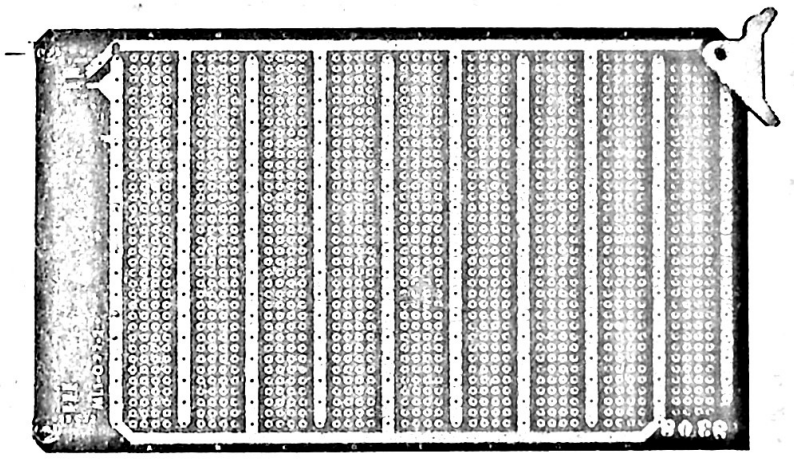
The CIM-611 Battery Charger Board mounts directly on the CIM-610 Voltage Regulator Board and requires only a single +24 V_{DC} power supply. It monitors the state of discharge of the external system battery and automatically provides a fast or trickle charge as required. The use of the CIM-611 and an external battery in conjunction with the CIM-610 Voltage Regulator Board creates an effectively uninterruptable system power supply. See the CIM-610/611 Hardware Reference Manual (#420306590-001) for a complete description of the CIM-610 Voltage Regulator Board and CIM-611 Battery Charger Board.

Functional Description

The CIM-611 Battery Charger Board mounts directly on the CIM-610 Voltage Regulator Board, and all connections to the CIM-611 are made through the CIM-610. The CIM-611 charges the external system battery, automatically adjusting the charge current according to the battery's state of discharge.

Circle DATA UPDATE No. 114300

CIM™-630 Prototyping Board



- **Permits addition of user-designed circuitry to a CIMBUS™ system**
- **Capacity for 32 16-pin DIPs**
- **Plugs directly into CIM-602/604 card cages**

Product Overview

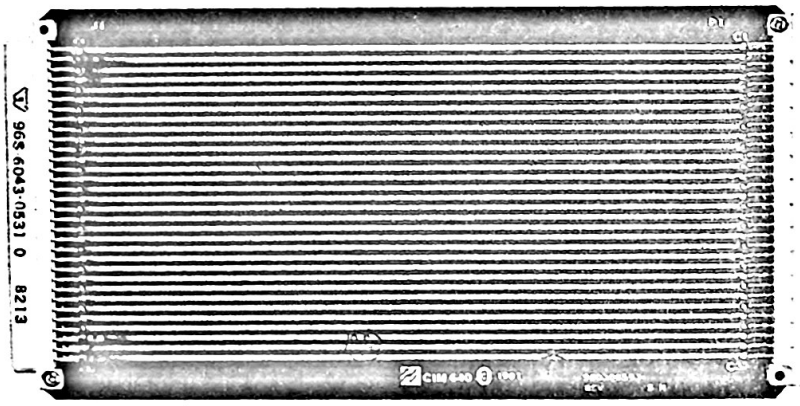
The CIM-630 Prototyping Board is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS™ NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-630 Prototyping Board, with a capacity of up to 32 16-pin DIPs, is a convenient, economical way for CIMBUS system users to include their own custom-designed circuitry. Completely compatible with the CIM-602/604 card cages, it plugs directly into the user's system.

Physical Description

The CIM-630 Prototyping Board accepts up to 32 16-pin DIPs or an equivalent mix of 14-, 16-, 18-, 22-, 24-, 28-, and 40-pin configurations. It has a pin-in-socket DIN 41612 connector built in, and plugs directly into the CIM-602/604 card cages.

CIM™-640 Extender Board



- **Complete access to a CIMBUS™ board for troubleshooting or debugging**
- **Power isolation allows removal/insertion of boards without loss of data or functions as well as current measurement in a powered system**
- **Easily accessible test points for fast examination of bus and control signals**

Product Overview

The CIM-640 Extender Board is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS™ NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

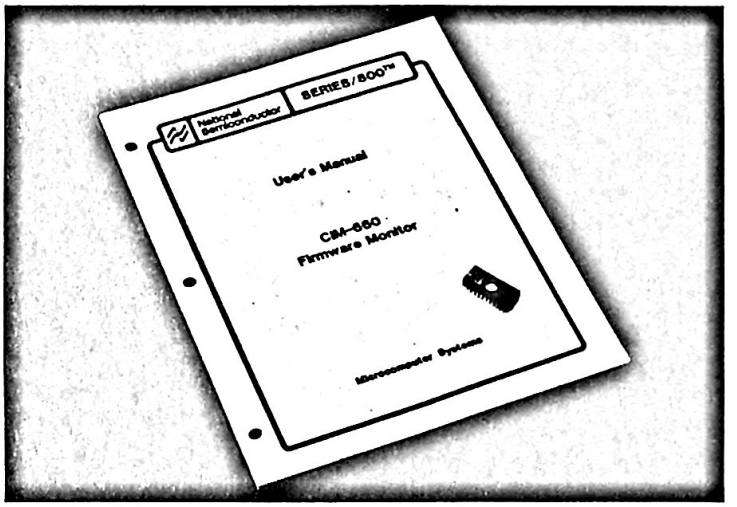
The CIM-640 Extender Board provides a means of extending CIMBUS boards away from the CIM-602/604 card cage to permit testing and debugging. Test points for examining bus and control signals are easily accessible, and the power lines contain jumpered openings for power removal at the extender board.

Physical Description

The CIM-640 Extender Board offers the SERIES/800 user the means to extend boards beyond the card cage for testing and debugging. Test points for bus and control signals are easily accessible.

In addition, the power traces on the CIM-640 have jumpered openings so that user can remove power at the board under examination rather than having to power down an entire system. The jumpered points in the power traces can also be used to insert instrumentation to measure the current to a board under power.

CIM™-660 Firmware Monitor



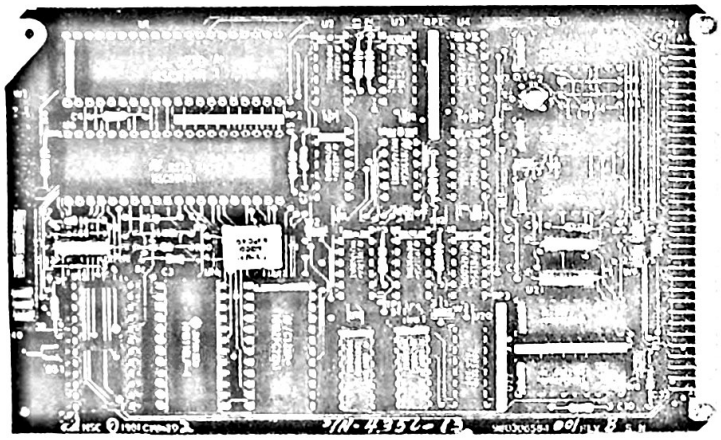
- **Single-chip system monitor for CIM-800 boards**
- **Display contents of memory or processor registers**
- **Modify contents of memory or processor registers**
- **Modify user programs dynamically**
- **Move blocks of data**
- **Perform hexadecimal arithmetic**
- **Search memory for specified data byte**
- **Execute user programs from monitor**
- **Insert breakpoints in user programs**
- **Input or output a byte of data**
- **Resides in a single NMC27C16 EPROM**

Product Overview

The CIM-660 Firmware Monitor is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS™ NSC800™ microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS™, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-660 Firmware Monitor is a single-chip (EPROM) system monitor that plugs into a socket provided on the CIM-800 Series Boards. Containing a complete software system, the CIM-660 provides the user all the functions usually associated with a microcomputer system monitor or debugging program and allows interactive program modification, testing, and execution.

CIM™-802
Industrial Microcomputer



- NSC800™-based computer board
- P²CMOS™ technology gives NMOS performance at CMOS power consumption levels
- NSC800 CPU—more than 158 instruction types programmable in Z80® code
- 2 MHz operation in harsh environments
- −40°C to +85°C (−40°F to +185°F) operating temperature range
- Battery backup/operation
- 2 16-bit counters/timers with prescalers
- 16 programmable I/O lines
- System-level fail-safe timer
- 2K bytes static RAM; 2K or 4K bytes PROM
- 12 vectored interrupts
- Built solely with components burned in to A+ levels

Product Overview

The CIM™-802 Microcomputer Board is a member of the SERIES/800™ line of CMOS Industrial Microcomputers (CIM) from National Semiconductor Corporation. SERIES/800 is a complete family, including CPU, memory expansion, and digital and analog I/O boards. Also included is a real-time, multitasking operating system, BLMX-80C. The line uses the P²CMOS™ NSC800 microprocessor, which combines the benefits of the execution speeds of NMOS microprocessors with the power dissipation and environmental characteristics of CMOS, and executes the Z80® instruction set. The complete line is compatible with the CIMBUS™, a documented scheme for board interconnection (see the CIMBUS specification). The CMOS technology employed, combined with the single-wide Eurocard form factor of the boards, makes the SERIES/800 line appropriate for many applications in harsh environments, such as numeric machine control, pipeline monitoring and control, robotics, industrial instrumentation, and uninterruptable power supplies.

The CIM-802 is the board level computer that is the heart of the SERIES/800 CMOS Industrial Microcomputer board line. Featuring NSC's P²CMOS technology, this computer provides highly reliable performance over a wide range of harsh environmental conditions at low power consumption, and is eminently suitable for remote station and process control applications.

National Semiconductor

November 1982

COP440R/COP2440R Piggyback-EPROM Microcontroller

General Description

The COP440R/COP2440R Piggyback-EPROM microcontrollers are members of the COPS™ family. The COP440R and COP2440R devices are identical to the COP440 and COP2440, respectively, except that the program ROM has been removed. In place of the ROM, each device package incorporates the circuitry and socket to accomodate the Piggyback-EPROM.

The socket provided on the package accepts an MM2716 or NMC27C16. Each part is a complete microcontroller system with CPU, RAM, I/O, and EPROM sockets provided in a single 40-pin package. In a system, the Piggyback device will perform exactly as its mask-programmed equivalent.

The complete package allows field test of a system in its final electrical and mechanical configuration. This important benefit facilitates development and debug of a COP400 program prior to masking of a production part.

These devices are also economical in low and medium volume applications or when the program may change.

Features

- Exact equivalent of the COP440/COP2440
- Socket and interface for industry standard EPROMS
- Two independent processors (COP2440)
- Dual CPU simplifies task partitioning—easy to program (COP2440)
- MICROWIRE™
- Enhanced, more powerful instruction set
- 160 × 4 RAM, addresses up to 2k × 8 ROM
- MICROBUS™ compatible
- Zero-crossing detect circuitry
- True multi-vectored interrupt from four selectable sources (plus restart)
- Four-level subroutine stack for each processor (in RAM)
- 4μs execution time per processor (non-overlapping)
- Single supply operation (4.5V–5.5V)
- Programmable time-base counter for real-time processing
- Software/hardware compatible with other members of COP400 family

TRI-STATE® is a registered trademark of National Semiconductor Corp.
COPS™, MICROWIRE™, and MICROBUS™ are trademarks of National Semiconductor Corp.

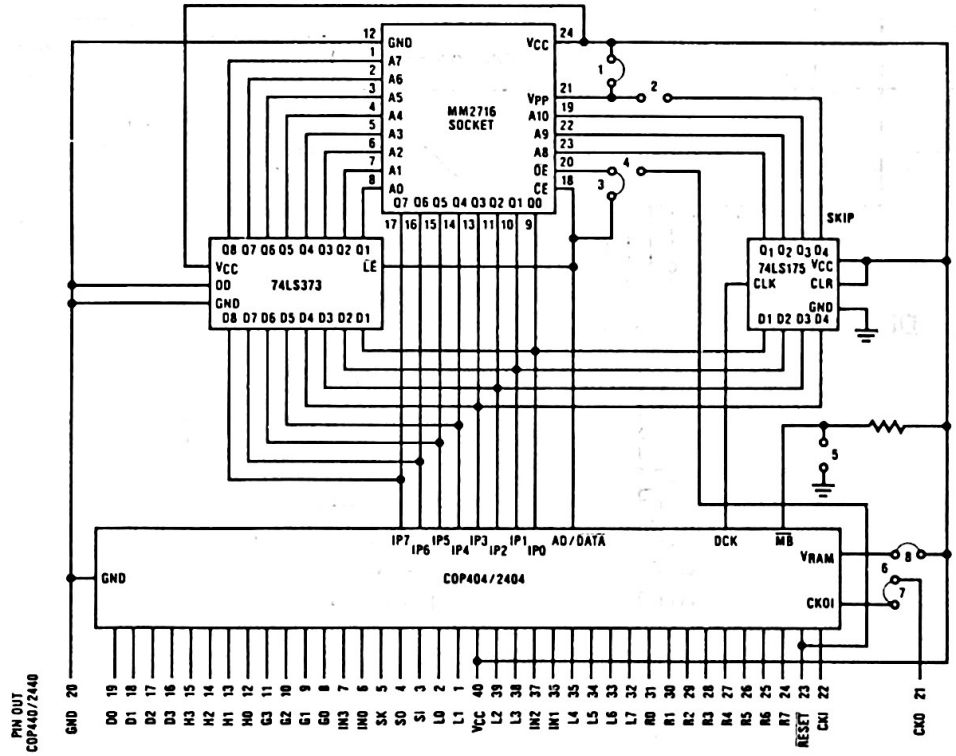


FIGURE 1. COP440R/COP2440R Block Diagram

Circle DATA UPDATE No. 101989

National Semiconductor

October 1982

DAC1280A, DAC1280 12-Bit Digital-to-Analog Converters

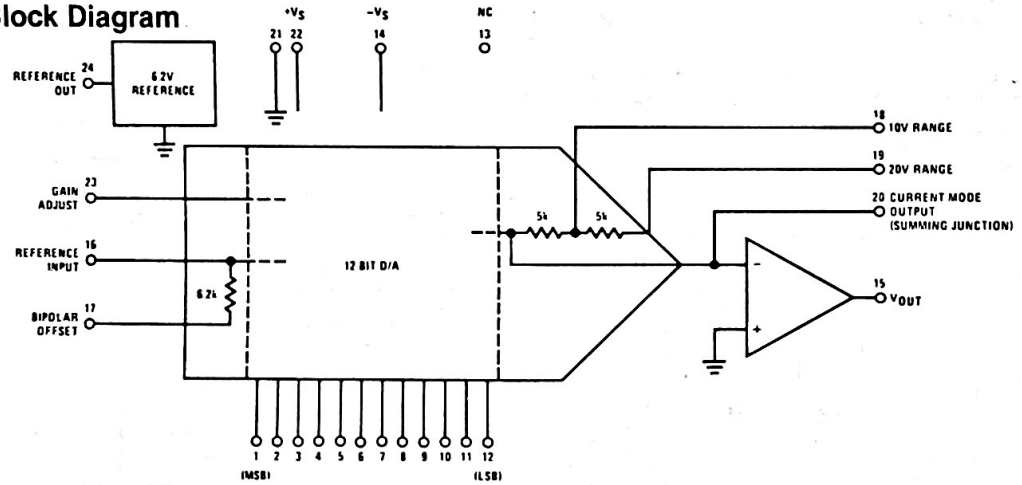
General Description

The DAC1280 series is a family of precision, low cost, fully self-contained digital-to-analog converters. The devices include 12 precision current switches, a 12-bit thin film resistor network, output amplifier, buffered internal reference, and several precision resistors, which allow the user to tailor his system needs to accommodate a variety of bipolar and unipolar output voltage and current ranges. Logic inputs are TTL and CMOS compatible, and are complementary binary (CBI) format. In all instances, a logic low (≤ 0.8V) turns a given bit ON, and a logic high (≥ 2V) turns a given bit OFF. Internally supplied resistor options provide low drift bipolar output voltage ranges of ± 2 5V, ± 5V, ± 10V, and unipolar ranges of 0V to 5V or 0V to 10V. Current mode output is 0 mA to 2 mA.

Features

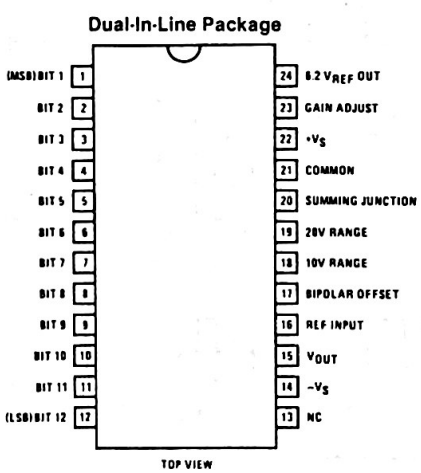
- Completely self-contained with internal reference and output amplifier
- High reliability exact replacement for DAC80-CBI-V or DAC80Z-CBI-V
- ± 1/2 LSB linearity max over 0°C to 70°C temperature range for DAC1280A
- ± 2.5V, ± 5V, ± 10V, 0V to 5V, 0V to 10V voltage outputs
- 0 mA to 2 mA current output
- Fast settling time: 300 ns current mode; 2.5 μs voltage mode
- Standard 24-pin IC package
- Low cost
- TTL CMOS compatible binary input logic over temperature

Block Diagram



Connection Diagram

Dual-In-Line Package



National Semiconductor

December 1982

DM75S68/DM85S68 16 × 4 Edge Triggered Registers

General Description

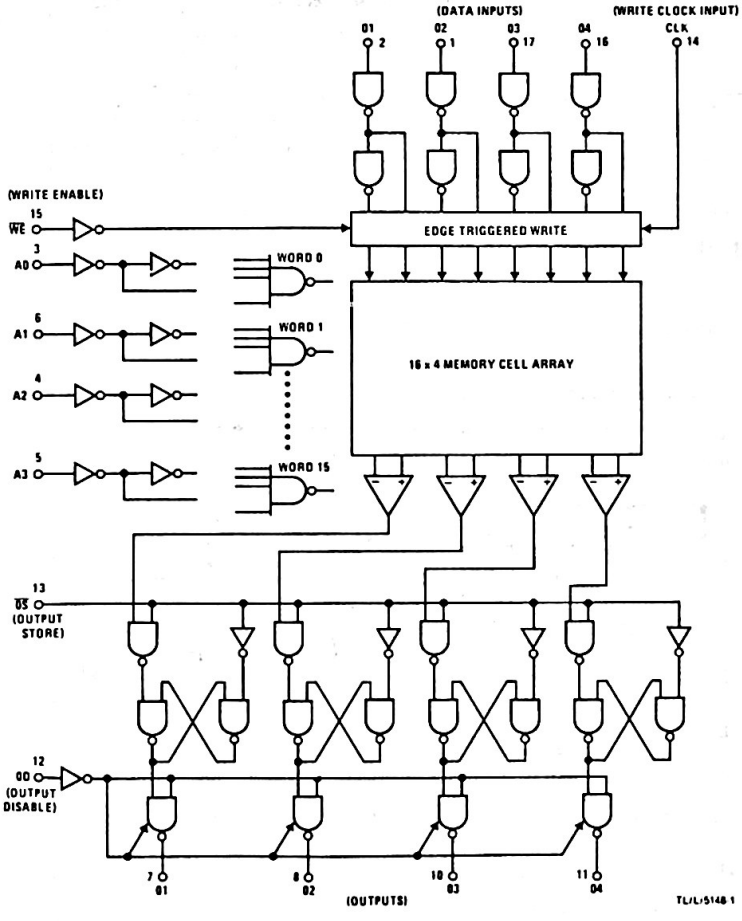
These Schottky memories are addressable "D" register files. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE* output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

Features

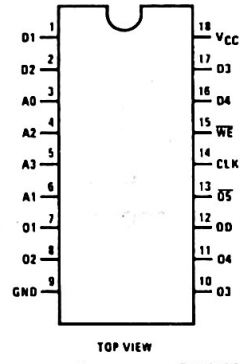
- On-chip output register
- PNP inputs reduce input loading
- Edge triggered write
- High speed—30 ns typ
- All parameters guaranteed over temperature
- TRI-STATE output
- Schottky-clamped for high speed
- Optimized for register stack applications
- Typical power dissipation—350 mW

Logic and Block Diagram



Connection Diagram

Dual-In-Line Package



TRI-STATE* is a registered trademark of National Semiconductor Corp.

National Semiconductor

December 1982

DM77/87S321 and DM77/87S421 (4,096 × 8) 32,768-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 4,096 words by 8-bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the eight outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

The DM77/87S321 and DM77/87S421 program the same as all other nonregistered PROMs from National.

Features

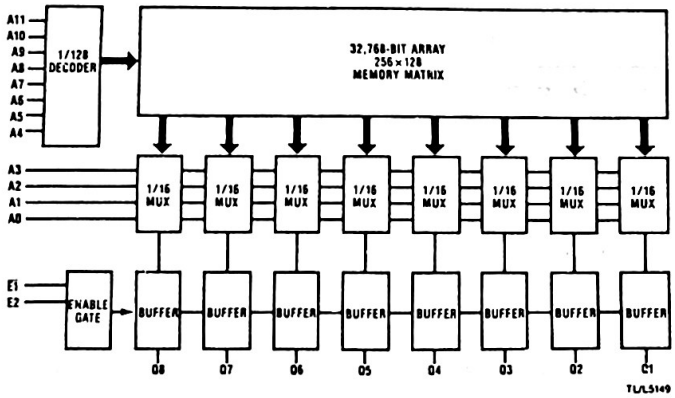
- Advanced fuse technology
- Schottky-clamped for high speed
  - Address access — 40ns typ.
  - Enable access — 20ns typ.
  - Enable recovery — 20ns typ.
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Generic programming.

	Military	Commercial	TRI-STATE®	Package
DM87S321		X	X	N,J
DM77S321	X		X	J
DM87S421		X	X	N,J*
DM77S421	X		X	J*

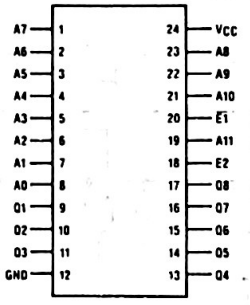
*Thin-Dip (0.3") package

TRI-STATE® is a registered trademark of National Semiconductor Corp.
TRI-SAFE™ is a trademark of National Semiconductor Corp.

Block and Connection Diagrams



TL/L5149



TL/L5149

Circle DATA UPDATE No. 102868

National Semiconductor

PRELIMINARY
October 1982

DM77S401/DM87S401, DM77S402/DM87S402 First-In, First-Out (FiFo) 64 x 4, 64 x 5 Serial Memories

General Description

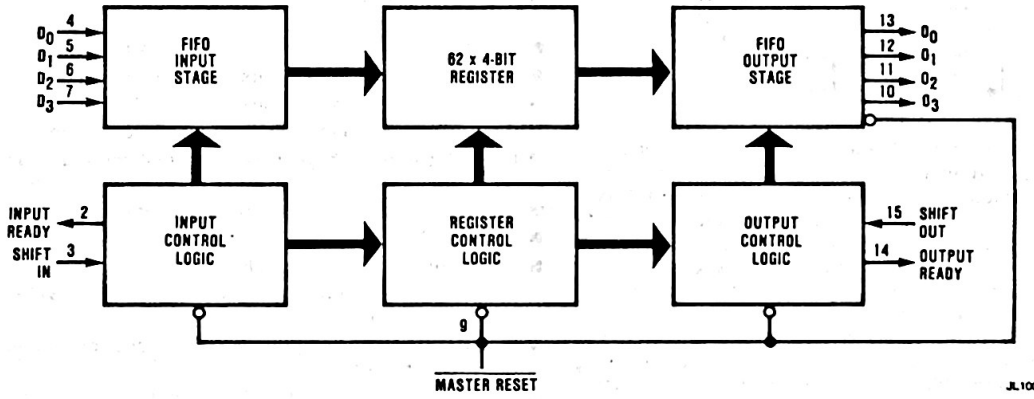
The DM77S401 is an expandable "fall-through" type high-speed First-in, First-out (FiFo) memory organized in 64-word by 4-bit, and 64-word by 5-bit structures respectively. A 20 MHz data rate allows usage in high-speed disc or tape controllers as well as PCM and communications buffer applications.

Features

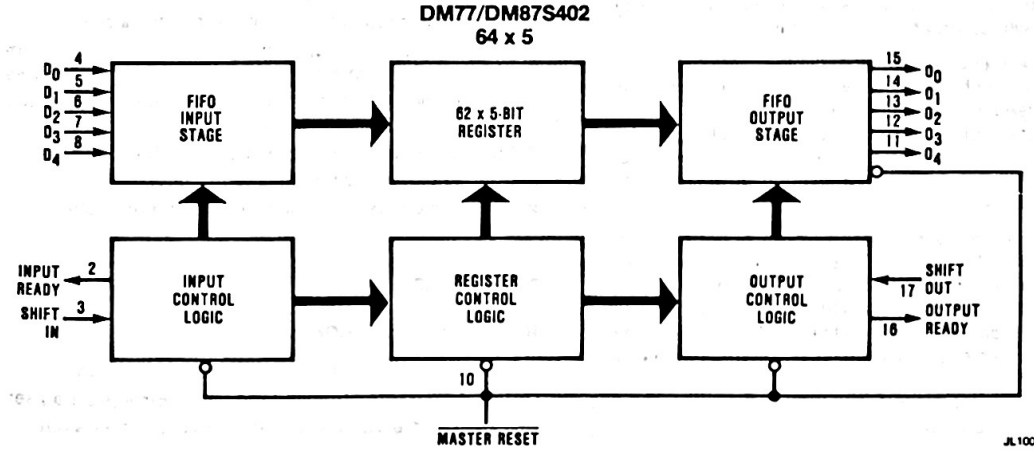
- 20 MHz shift in, shift out
- TTL inputs and outputs
- Inputs and outputs are symmetrically placed on package
- Easily expandable word and bit dimensions
- Either synchronous or asynchronous operation
- Fairchild F3341 MOS FiFo pin compatible but 20 times faster!
- Twice as fast as MMI's 57/67401
- Choice of 4-bit or 5-bit data width

Block Diagrams

DM77/DM87S401
64 x 4



DM77/DM87S402
64 x 5



Circle DATA UPDATE No. 102860

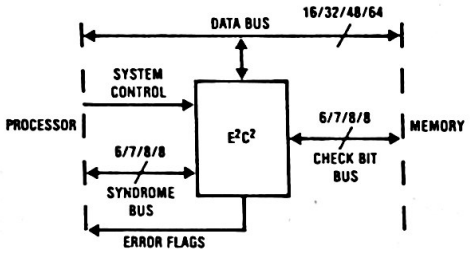
National Semiconductor

November 1982

DP8400 — E^2C^2 Expandable Error Checker and Corrector

General Description

The DP8400 Expandable Error Checker and Corrector (E^2C^2) aids system reliability and integrity by detecting errors in memory data and correcting single or double-bit errors. The E^2C^2 data I/O port sits across the processor-memory data bus as shown, and the check bit I/O port connects to the memory check bits. Error flags are provided, and a syndrome I/O port is available. Fabricated using high speed Schottky technology in a 48-pin dual-in-line package, the DP8400 has been designed such that its internal delay times are minimal, maintaining maximum memory performance.



For a 16-bit word, the DP8400 monitors data between the processor and memory, with its 16-bit bidirectional data bus connected to the memory data bus. The DP8400 uses an encoding matrix to generate 6 check bits from the 16 bits of data. In a WRITE cycle, the data word and the corresponding check bits are written into memory. When the same location of memory is subsequently read, the E^2C^2 generates 6 new check bits from the memory data and compares them with the 6 check bits read from memory to create 6 syndrome bits. If there is a difference (causing some syndrome bits to go high), then that memory location contains an error and the DP8400 indicates the type of error with 3 error flags. If the error is a single-bit error, the DP8400 will automatically correct it.

The DP8400 is easily expandable to other data configurations. For a 32-bit data bus with 7 check bits, two DP8400s can be used in cascade with no other ICs. Three DP8400s can be used for 48 bits, and four DP8400s for 64 data bits, both with 8 check bits. In all these configurations, single and double-error detection and single-error correction are easy to implement.

When the memory is more unreliable, or better system integrity is preferred, then in any of these configurations, double-error correction can be performed. One approach requires a further memory WRITE-READ cycle using complemented data and check bits from the DP8400. If at least one of the two errors is a hard error, the DP8400 will correct both errors. This implementation requires no more memory check bits or DP8400s than the single-error correct configurations.

The DP8400 has a separate syndrome I/O bus which can be used for error logging or error management. In addition, the DP8400 can be used in BYTE-WRITE applications (for up to 72 data bits) because it has separate byte controls for the data buffers. In 16 or 32-bit systems, the DP8400 will generate and check system byte parity, if required, for integrity of the data supplied from or to the processor. There are three latch controls to enable latching of data in various modes and configurations.

Operational Features

- Fast single and double-error detection
- Fast single-error correction
- Double-error correction after catastrophic failure with no additional ICs or check bits
- Functionally expandable to 100% double-error correct capability
- Functionally expandable to triple-error detect
- Directly expandable to 32 bits using 2 DP8400s only
- Directly expandable to 48 bits using 3 DP8400s only
- Directly expandable to 64 bits using 4 DP8400s only
- Expandable to and beyond 64 bits in fast configuration with extra ICs
- 3 error flags for complete error recording
- 3 latch enable inputs for versatile control
- Byte parity generating and checking
- Separate byte controls for outputting data in BYTE-WRITE operation
- Separate syndrome I/O port accessible for error logging and management
- On-chip input and output latches for data bus, check bit bus and syndrome bus
- Diagnostic capability for simulating check bits
- Memory check bit bus, syndrome bus, error flags and internally generated syndromes available on the data bus
- Self-test of E^2C^2 on the memory card under processor control
- Full diagnostic check of memory with the E^2C^2
- Complete memory failure detectable
- Power-on clears data and syndrome input latches

Timing Features

16-BIT CONFIGURATION

WRITE Time: 35 ns from data-in to check bits valid
DETECT Time: 35 ns from data-in to Any Error (AE) flag set
CORRECT Time: 70 ns from data-in to correct data out

 BF/2183

National Semiconductor

November 1982

DP8409 Multi-Mode Dynamic RAM Controller/Driver

General Description

Dynamic memory system designs, which formerly required several support chips to drive the memory array, can now be implemented with a single IC. . . the DP8409 Multi-Mode Dynamic RAM Controller/Driver. The DP8409 is capable of driving all 16k and 64k Dynamic RAMs (DRAMs) as well as 256k DRAMs. Since the DP8409 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, the major performance disadvantage of multiple-chip memory drive and control.

The DP8409's 8 modes of operation offer a wide selection of DRAM control capabilities. Memory access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The DP8409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. All output drivers are capable of driving 500 pF loads with propagation delays of 25 ns. The DP8409 timing parameters are specified driving the typical load capacitance of 88 DRAMs, including trace capacitance.

The DP8409 has 3 mode-control pins: M2, M1, and M0, where M2 is in general $\overline{\text{REFRESH}}$. These 3 pins select 8 modes of operation. Inputs B1 and B0 in the memory access modes (M2 = 1), are select inputs which select one of four $\overline{\text{RAS}}$ outputs. During normal access, the 9 address outputs can be selected from the Row Address Latch or the Column Address Latch. During refresh, the 9-bit on-chip refresh counter is enabled onto the address bus and in this mode all $\overline{\text{RAS}}$ outputs are selected, while $\overline{\text{CAS}}$ is inhibited.

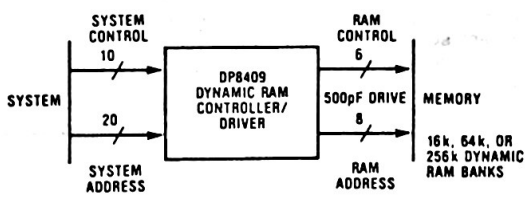
The DP8409 can drive up to 4 banks of DRAMs, with each bank comprised of 16k's, 64k's, or 256k's. Control signal outputs $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ are provided with the same drive capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and the multiplexed addresses can be connected to all of the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the data outputs in TRI-STATE®. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from.

Operational Features

- All DRAM drive functions on one chip — minimizes skew on outputs, maximizes AC performance
- On-chip capacitive-load drives (specified to drive up to 88 DRAMs)
- Drives directly all 16k, 64k, and 256k DRAMs
- Capable of addressing 64k, 256k, or 1M words
- Propagation delays of 25 ns typical at 500 pF load
- $\overline{\text{CAS}}$ goes low automatically after column addresses are valid if desired
- Auto Access mode provides $\overline{\text{RAS}}$, row to column select, then $\overline{\text{CAS}}$ automatically and fast
- $\overline{\text{WE}}$ follows $\overline{\text{WIN}}$ unconditionally—offering READ, WRITE or READ-MODIFY-WRITE cycles
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255, or 511)
- End-of-Count indicated by RF I/O pin going low at 127, 255, or 511
- Low input on RF I/O resets 9-bit refresh counter
- $\overline{\text{CAS}}$ inhibited during refresh cycle
- Fall-through latches on address inputs controlled by ADS
- TRI-STATE outputs allow multi-controller addressing of memory
- Control output signals go high-impedance logic "1" when disabled for memory sharing
- Power-up: counter reset, control signals high, address outputs TRI-STATE, and End-of-Count set to 127

Mode Features

- 8 modes of operation: 3 access, 3 refresh, and 2 set-up
- 2 externally controlled modes: 1 access and 1 refresh (Modes 0, 4)
- 2 auto-access modes $\overline{\text{RAS}} \rightarrow \text{R}/\overline{\text{C}} \rightarrow \overline{\text{CAS}}$ automatic, with $t_{RAH} = 20$ or 30 ns minimum (Modes 5, 6)
- Auto-access mode allows Hidden Refreshing (Mode 5)
- Forced Refresh requested on RF I/O if no Hidden Refresh (Mode 5)
- Forced Refresh performed after system acknowledge of request (Mode 1)
- Automatic Burst Refresh mode stops at End-of-Count of 127, 255, or 511 (Mode 2)
- 2 All-$\overline{\text{RAS}}$ Access modes externally or automatically controlled for memory initialization (Modes 3a, 3b)
- Automatic All-$\overline{\text{RAS}}$ mode with external 8-bit counter frees system for other set-up routines (Mode 3a)
- End-of-Count value of Refresh Counter set by B1 and B0 (Mode 7)



National Semiconductor

November 1982

DS8908 AM/FM Digital Phase-Locked Loop Frequency Synthesizer

General Description

The DS8908 is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, an operational amplifier, a 120 MHz ECL/I^2L dual modulus programmable divider, and a 19-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necessary division codes for each frequency, and logic state information for radio function inputs/outputs.

A 3.96 MHz pierce oscillator and divider chain generate a 1.98 MHz external controller clock, a 20 kHz, 10 kHz, 9 kHz, and 1 kHz reference signals, and a 50 Hz time-of-day signal. The oscillator and divider chain are sourced by the V_{CCM} pin thus providing a low power controller clock drive and time-of-day indication when the balance of the PLL is powered down.

The 21-bit serial data stream is transferred between the frequency synthesizer and the controller via a 3-wire bus system comprised of a data line, a clock line, and an enable line.

The first 2 bits in the serial data stream address the synthesizer thus permitting other devices such as display drivers to share the same bus. The next 14 bits are used for the PLL (N + 1) divide code. The 15th bit is used internally to select the AM or FM local oscillator input. A high level on this bit enables the FM input and a low level enables the AM input. The 16th and 17th bits are used to select one of the 4 reference frequencies. The 18th and 19th bits are connected via latches to open collector outputs. These outputs can be used to drive radio functions such as gain, mute, AM, FM, or charge pump current source levels.

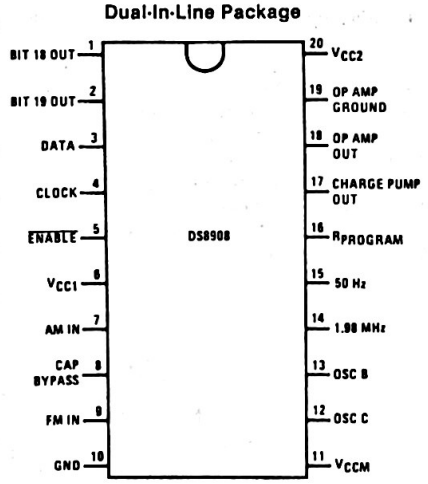
The PLL consists of a 14-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p + 1) prescaler, a high speed charge pump, and an operational amplifier. The programmable divider divides by (N + 1), N being the number loaded into the shift register. The programmable divider is clocked through a ÷7/8 prescaler by the AM input or through a ÷63/64 prescaler by the FM input. The AM input will work at frequencies up to 15 MHz, while the FM input works up to 120 MHz. The VCO can be tuned with a frequency resolution of either 1 kHz, 9 kHz, 10 kHz, or 20 kHz.The buffered AM and FM inputs are self-biased and can be driven directly by the VCO through a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator. The high speed charge pump consists of a switchable constant current source and sink. The charge pump can be programmed to deliver from 75 μA to 750 μA of constant current by connection of an external resistor from pin $R_{PROGRAM}$ to ground or the open collector bit outputs. Connection of programming resistors to the bit outputs enables the controller to adjust the loop gain for the particular reference frequency selected. The charge pump will source current if the VCO frequency is high and sink current if the VCO frequency is low. The low noise operational amplifier provided has a high impedance JFET input and a large output voltage range. The op amp's negative input is common with the charge pump output and its positive input is internally biased.

Features

- Uses inexpensive 3.96 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of either 10 kHz or 20 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for time-of-day reference driven from separate low power V_{CCM}
- 2 open collector buffered outputs for controlling various radio functions or loop gain
- Separate AM and FM inputs; AM input has 15 mV (typical) hysteresis
- Programmable charge pump current sources enable adjustment of system loop gain
- Operational amplifier provides high impedance load to charge pump output and a wide voltage range for the VCO input

Connection Diagram

Dual-In-Line Package



TOP VIEW

December 1982

National Semiconductor

DTSW-500 Digitalker™ Vocabulary Selection System

Product Description

The DTSW-500 Digitalker™ Vocabulary Selection System (DVSS) is a CP/M software package which provides 500 highly intelligible English words in a male speaking voice. These words are intended for users of National Semiconductor's Digitalker MM54104 Speech Processor Chip. The package provides complete menu driven software that allows users to create speech PROMs containing a vocabulary of words, phrases, or sentences put together from the 500 words supplied.

The DVSS package consists of 2 floppy disks and a functional specification. The first disk contains the speech data archive and the second contains the system software. Both floppy disks are standard 8" single-sided, single density disks written in CP/M format.

In a typical application, a user would start by developing a vocabulary for his envisioned talking product. This vocabulary could be composed of a list of single words, phrases, or sentences. A CP/M file is created containing the vocabulary list using any CP/M based text editor or the editor provided with the DVSS. This vocabulary list is checked to assure that all words on the list are contained in the current archive. Missing or misspelled words are flagged and the user must then return to the text editor to make corrections.

The DVSS software creates what is called a work file for the vocabulary from an error-free vocabulary list. This work file can then be submitted to the ROM building routine. The output is a ROM image in one of two formats, either binary or Intellec hexadecimal. Either of these files in turn can be used to program PROMs.

In order to use the DVSS software, a user needs a computer system that runs CP/M and that can read two 8 inch single density, single sided CP/M formatted floppy disks simultaneously. The system must also include an 80 column by 24 line CRT. Otherwise, DVSS is a self contained software system.

The DVSS programs are easy to use. Menu selections guide the user through all program modules. A complete instruction manual and tutorial examples ensure that even a person unfamiliar with speech or programming will have little difficulty in producing vocabulary lists and speech PROMs.

The speech ROM images produced by the DVSS system will be nearly as memory efficient as speech ROMs produced at the National Semiconductor Speech Lab. The data rate for ROMs containing more than 50 words will be approximately 1200 bits per word. Smaller vocabularies result in slightly higher data rates.

Features

- Create your own speech ROMs
- Choose words from a large library
  - — 500 words to start
  - — Future library expansion
- Build sentences and phrases
- No previous knowledge of synthetic speech required
- Runs on most CP/M machines
- Easy to use menu driven program

Functional Description

THE SPEECH DATA ARCHIVE

The speech data disk supplied with the system contains 500 words. (See Table 3.) Each word stored on the floppy is a self-contained, stand-alone, playable entity. Adding further standard vocabulary or even custom words to the archive is a simple operation which is discussed in the software section below.

THE SOFTWARE

The DVSS software is a CP/M 2.2 applications program written in BDS C which will execute on most CP/M 2.2 compatible computers. The software requires the service of a CRT terminal. (Supported terminals are listed in Table 2.) The system manual explains how to add support for terminals which are not listed.

The entire program is operated by making menu-prompted choices. At every level of the program there is a "Help" option which provides on-line documentation of all available choices. The highest level menu selections (shown in Table 1) outline the basic functions of the software.

TABLE 1. The Top Level DVSS Menu

Digitalker Vocabulary Selection System

Quit
Help
Operate on Speech Data Archives
→ Prepare Vocabulary Lists
Build Speech Data ROM images
Program Speech Data EPROMs

Hit SPACE to move selector; hit RETURN to perform selection.

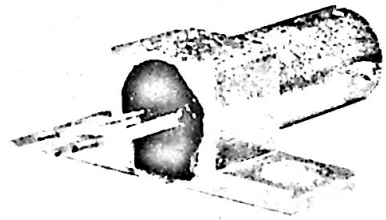
National Semiconductor

December 1982

FOE380B-1/FOE380B-2 Fiber-Optic Emitter

General Description

The FOE380B is a series of self-contained Gallium Aluminum Arsenide infrared emitters designed for data transmission via optical fibers with the female portion of the connector integral to the low profile cast metal housing. The FOE380B series is designed to mount directly to PC boards with 0.5" or greater board-to-board spacing. To ensure reliable and repeatable optical coupling with minimum source-to-fiber alignment losses, the package mates with the Amphenol™ micro bayonet connector. When used with the FOR361B series of Fiber-Optic Receivers, the system is ideal for data rates from DC to 10MBits/s NRZ.



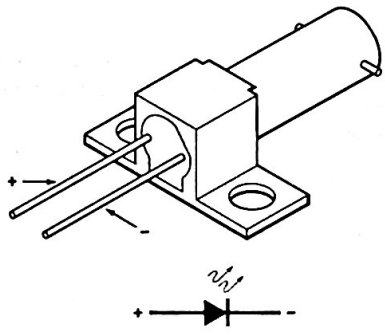
Features

- High efficiency 820nm emitter
- High-speed, fast response; 30ns
- Eliminates receptacle housing
- Lower total system cost
- Low profile—under 0.3"
- Quickly demountable Amphenol bayonet-type optical connector
- Efficient and reliable optical coupling
- Wavelength matched to minimum attenuation region of most glass fiber cables.

Applications

- Data communication networks
- Secure communications
- Peripheral control/communications
- Industrial machine control
- Video transmission
- FCC compliant interconnections

Connection Diagram



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Circle DATA UPDATE No. 104300

National Semiconductor

November 1982

FOR261F-1/FOR261F-2 Monolithic TTL Fiber-Optic Receiver

General Description

The FOR261F is a series of high-speed monolithic fiber-optic receivers accepting optical input and providing TTL outputs at NRZ data rates to 10 Mbits/s with either 15 or 20 μW of optical power. It is available in a short ferrule package which is compatible with Amphenol™ and AMP™ standard receptacles.

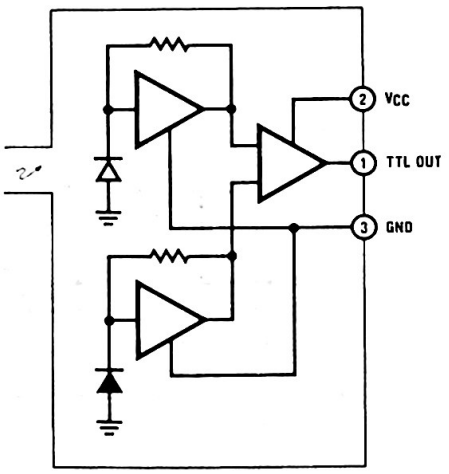
Features

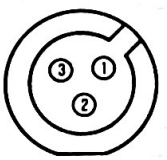
- Single +5V supply
- Optical input, TTL output
- 10 Mbits/s NRZ data rate with fanout of 10
- < 10^{-10} bit error rate
- Short ferrule package with 400 μM diameter optical port
- Compatible with AMP #227240-1 and Amphenol #905-135-5000 receptacle
- Temperature-compensated input
- DC coupled

Applications

- Data communications
- Optical modem
- Industrial machine control
- Peripheral control/communications

Equivalent Circuit and Connection Diagram





BOTTOM VIEW

TL/K/5099-1

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Circle DATA UPDATE No. 104315

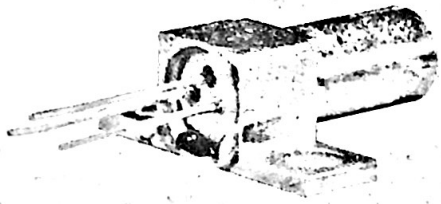
National Semiconductor

November 1982

FOR361B-1/FOR361B-2 Fiber-Optic Receiver

General Description

The FOR361B is a series of self-contained monolithic TTL-compatible receivers designed for data transmission via optical fibers with the female portion of the connector integral to the low profile cast metal housing. The FOR361B series is designed to mount directly to PC boards with 0.5" or greater board-to-board spacing. To ensure reliable and repeatable optical coupling with minimum source-to-fiber alignment losses, the package mates with the Amphenol™ micro bayonet connector. When used with the FOE380B series of Fiber-Optic Emitters, the system is ideal for data rates from DC to 10 MBits/s NRZ.



Features

- Single +5V supply
- Optical input, TTL output
- 10 MBits/s NRZ data rate
- $<10^{-10}$ bit error rate
- Low profile—under 0.3"
- Eliminates receptacle housing
- Quickly demountable Amphenol bayonet-type optical connector
- Efficient and reliable optical coupling
- Temperature compensated input

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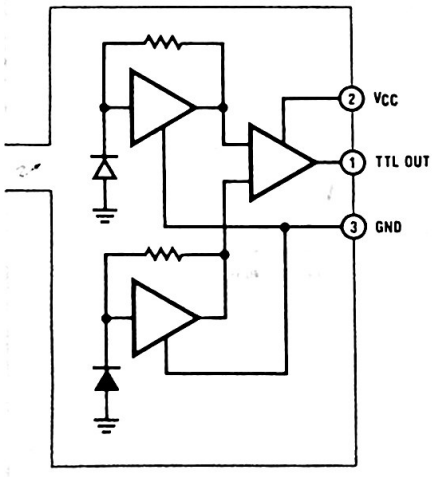
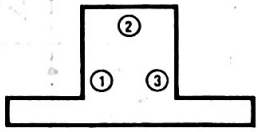
Applications

- Data communication networks
- Optical modem
- Industrial machine control
- Peripheral control/communications
- Secure communications
- Video transmission
- FCC compliant interconnections

Equivalent Schematic and Connection Diagram





Back View

Circle DATA UPDATE No. 104325

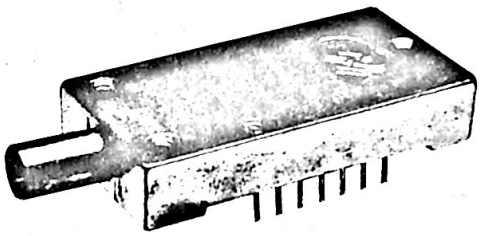
National Semiconductor

November 1982

FOT180B Fiber-Optic Transmitter

General Description

The FOT180B is a high-speed fiber-optic transmitter. It is designed for digital data transmission via optical fibers with data rates up to 20 MBits/s NRZ. The package includes the driver circuitry, optical light source, and female portion of the connector. The bayonet-type connector on the package simplifies and ensures reliable optical coupling with minimal source to fiber alignment losses. The low-profile metal package is ideal for direct PC board mounting with 0.5" board-to-board spacing. When used with the FOR100B fiber-optic receiver, the pair provides a complete optical data link with TTL compatible interfacing. Connectors are available from Amphenol™.



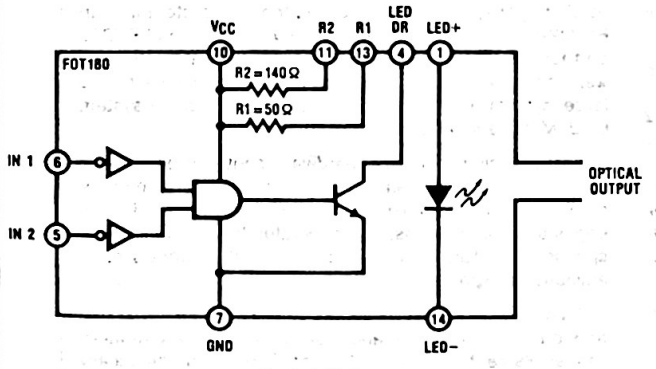
Features

- Single +5V supply
- DC to 20 Mbits/s NRZ data rate
- Pin selectable optical output power
- LED built-in
- CMOS/TTL compatibility
- Data and enable inputs
- Quickly demountable Amphenol bayonet-type optical connector
- 14-pin low profile package (0.3") for direct PC board mounting
- Open collector output driver

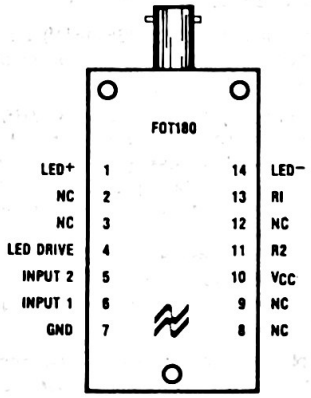
Applications

- Data communication networks
- Secure communications
- Peripheral control/communication
- Industrial machine control
- T1 and T2 telecom digital links
- Optical modems
- Video transmission

Schematic and Connection Diagram



Case is isolated.



TOP VIEW

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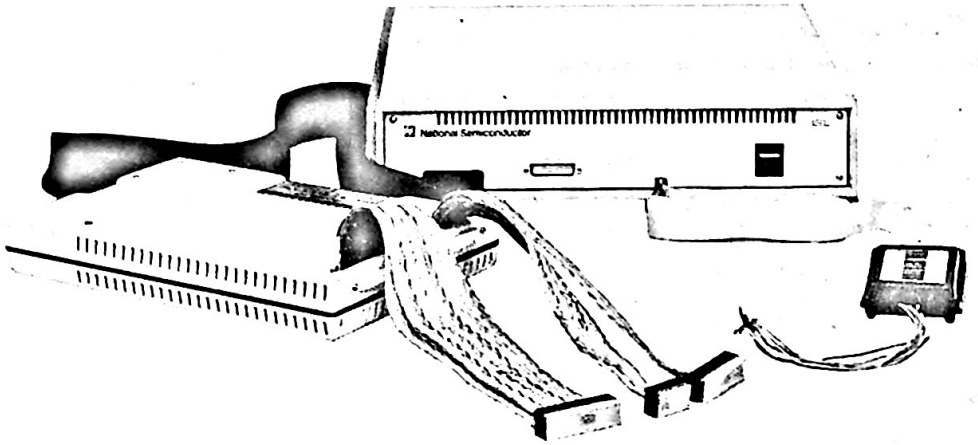
Circle DATA UPDATE No. 540095

National Semiconductor

October 1982

ISE/16™ NS16000 Family In-System Emulator



Features

- Operation up to 6 MHz
- Emulation of NS16032 Central Processing Unit, NS16082 Memory Management Unit, NS16201 Timing Control Unit
- Host resident high level language and assembly language symbolic debugger
- Generalized event driven system
- Memory mapping, up to 30K bytes
- Write protection/detection of 2K byte memory blocks
- Program flow tracing, up to 255 non-sequential fetches
- Complete bus activity trace
- Qualified tracing
- Pre-, post-, or center- triggering on trace
- Count-down event counter
- Count-up execution timer/counter
- Supports memory management unit functions
- Runs on VAX/11 (VMS) host
- Hierarchical help facility (on-line manual)
- Self-diagnostic

1. Product Description

The NS16032 In-System Emulator (ISE/16™) is a powerful tool for both hardware and software development of NS16032 microprocessor-based products.

When used with a host system such as VAX (VMS), ISE/16 emulates a complete NS16000 chip set. This chip set includes the 16032 Central Processing Unit (CPU), the 16082 Memory Management Unit (MMU), and the 16201 Timing Control Unit (TCU). ISE/16 allows users to test and debug both hardware and software in their own hardware environment. ISE/16 operates in either of two modes: emulation mode, when ISE/16 is actually running the user's program, or monitor mode, when ISE/16 is communicating with the user via the host system.

ISE/16 is a complete unit, including an internal clock oscillator and 30K bytes of RAM. With ISE/16, users can easily stop emulation and examine the contents of CPU registers, slave processor registers, and memory.

ISE/16 consists of the ISE™ hardware, the ISE monitor, and a host-dependent debugger (IDBG16).

ISE/16 hardware is the circuitry required for emulation of a user's target system. It interfaces to the host system with an RS232-compatible serial link and provides a second RS232 port for an optional terminal connection. The ISE/16 hardware also has three target cables for connections to the target system. The target cables plug into the target system CPU, MMU, and TCU sockets.

The ISE monitor is the ISE hardware control program that monitors the host system serial data link. The ISE monitor receives monitor commands from the host system, acknowledges these commands, and generates the appropriate responses. The ISE monitor also controls the target system emulation program.

IDBG16 is the interactive debugger program for ISE/16. It runs on the host system and makes the host system facilities available to the ISE/16 user. IDBG16 automatically translates commands entered at a host system terminal to the equivalent ISE monitor commands, and communicates with the ISE monitor via the serial data link.

National Semiconductor

October 1982

LM194/LM394 Supermatch Pair

General Description

The LM194 and LM394 are junction isolated ultra well-matched monolithic NPN transistor pairs with an order of magnitude improvement in matching over conventional transistor pairs. This was accomplished by advanced linear processing and a unique new device structure.

Electrical characteristics of these devices such as drift versus initial offset voltage, noise, and the exponential relationship of base-emitter voltage to collector current closely approach those of a theoretical transistor. Extrinsic emitter and base resistances are much lower than presently available pairs, either monolithic or discrete, giving extremely low noise and theoretical operation over a wide current range. Most parameters are guaranteed over a current range of 1μA to 1 mA and 0V up to 40V collector-base voltage, ensuring superior performance in nearly all applications.

To guarantee long term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation due to reverse biased emitter current—the most common cause of field failures in matched devices. The parasitic isolation junction formed by the diodes also clamps the substrate region to the most negative emitter to ensure complete isolation between devices.

The LM194 and LM394 will provide a considerable improvement in performance in most applications requiring a closely matched transistor pair. In many cases, trimming can be eliminated entirely, improving reliability and decreasing costs. Additionally, the low noise and high gain make this device attractive even where matching is not critical.

The LM194 and LM394/LM394B/LM394C are available in an isolated header 6-lead TO-5 metal can package. The LM394/LM394B/LM394C are also offered in an 8-lead DIP. The LM194 is identical to the LM394 except for tighter electrical specifications and wider temperature range.

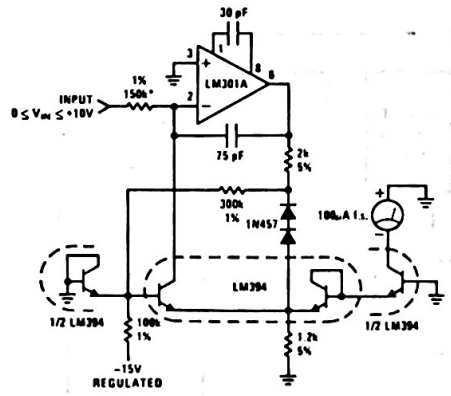
Features

- Emitter-base voltage matched to 50μV
- Offset voltage drift less than 0.1μV/°C
- Current gain (h_{FE}) matched to 2%
- Common-mode rejection ratio greater than 120 dB
- Parameters guaranteed over 1μA to 1 mA collector current
- Extremely low noise
- Superior logging characteristics compared to conventional pairs
- Plug-in replacement for presently available devices

Typical Applications

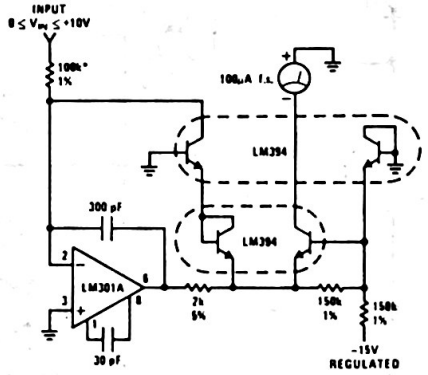
Low Cost Accurate Square Root Circuit

$I_{OUT} = 10^{-5} \cdot \sqrt{10\,V_{IN}}$



Low Cost Accurate Squaring Circuit

$I_{OUT} = 10^{-6}\,(V_{IN})^2$



*Trim for full scale accuracy

Circle DATA UPDATE No. 106614

National Semiconductor

October 1982

LM1949 Injector Drive Controller

General Description

The LM1949 linear integrated circuit serves as an excellent control of fuel injector drive circuitry in modern automotive systems. The IC is designed to control an external power NPN Darlington transistor that drives the high current injector solenoid. The current required to open a solenoid is several times greater than the current necessary to merely hold it open; therefore, the LM1949, by directly sensing the actual solenoid current, initially saturates the driver until the "peak" injector current is four times that of the idle or "holding" current (*Figure 3-Figure 7*). This guarantees opening of the injector. The current is then automatically reduced to the sufficient holding level for the duration of the input pulse. In this way, the total power consumed by the system is dramatically reduced. Also, a higher degree of correlation of fuel to the input voltage pulse (or duty cycle) is achieved, since opening and closing delays of the solenoid will be reduced.

Normally powered from a 5-volt ±10% supply, the IC is typically operable over the entire temperature range (-55°C to +125°C ambient) with supplies as low as 3 volts. This is particularly useful under "cold crank" conditions when the battery voltage may drop low enough to deregulate the 5-volt power supply.

The LM1949 is available in the plastic miniDIP, (contact factory for other package options).

Features

- Low voltage supply (3V-5.5V)
- 22mA output drive current
- No RFI radiation
- Adaptable to all injector current levels
- Highly accurate operation
- TTL/CMOS compatible input logic levels
- Short circuit protection
- High impedance input
- Externally set holding current, I_H
- Internally set peak current (4 x I_H)
- Externally set time-out
- Can be modified for full switching operation
- Available in plastic 8-pin miniDIP

Applications

- Fuel injection
- Throttle body injection
- Solenoid controls
- Air and fluid valves
- DC motor drives

Typical Application Circuit

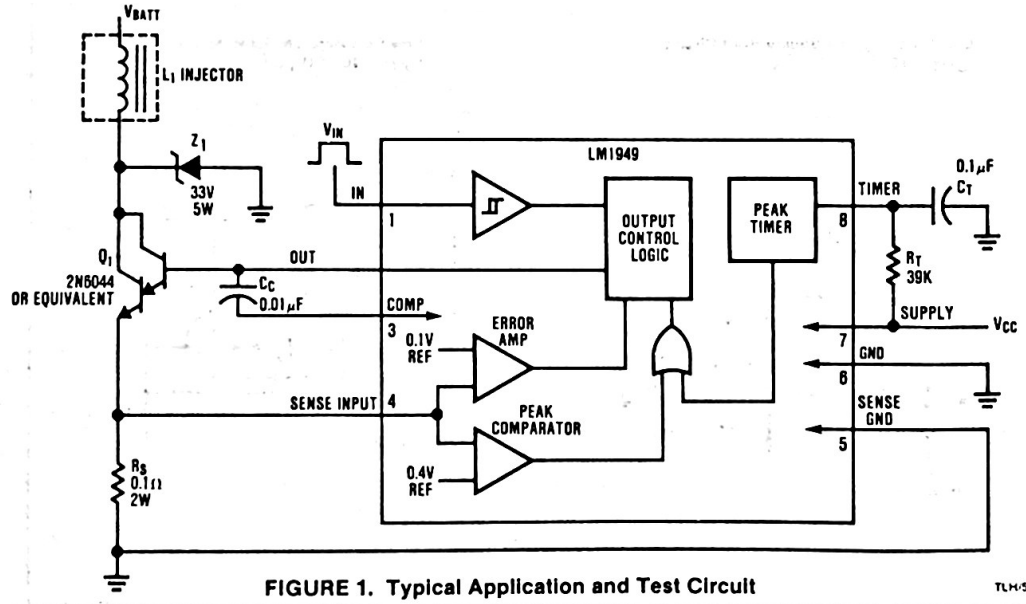


FIGURE 1. Typical Application and Test Circuit

TL/H/5062-1

National Semiconductor

PRELIMINARY
November 1982

LP165/LP365 Micropower Programmable Quad Comparator

General Description

The LP165 series consists of four independent voltage comparators. The comparators can be programmed, four at the same time, for various supply currents, input currents, response times and output current drives. This is accomplished by connecting a single resistor between the V_{CC} and I_{SET} pins.

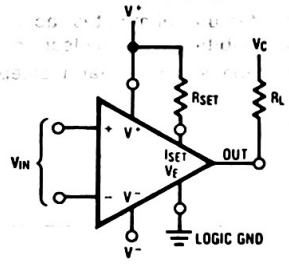
These comparators can be operated from split power supplies or from a single power supply over a wide range of voltages. The input can sense signals at ground level even with single supply operation. The unique output NPN transistor stages are uncommitted to either power supply. They can be connected directly to various logic system supplies so that they are highly flexible to interface with various logic families.

Application areas include battery power circuits, threshold detectors, zero crossing detectors, simple serial A/D converters, VCO, multivibrators, voltage converters, power sequencers, and high performance V/F converters, and RTD linearization.

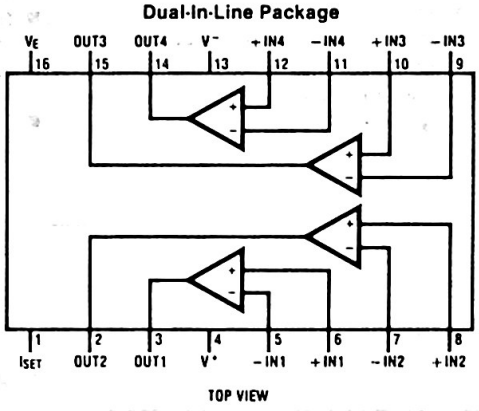
Features

- Single programming resistor to tailor power consumption, input current, speed and output current drive capability
- Wide single supply voltage range or dual supplies (4 V_{DC} to 36 V_{DC} or ± 2.0 V_{DC} to ± 18 V_{DC})
- Low supply current drain (10 μA) and low power consumption (10 μW/comparator)@I_{SET} = 0.5 μA V_{CC} = 5 V_{DC}
- Uncommitted output stage — selectable output levels
- Output directly compatible with DTL, TTL, CMOS, MOS or other special logic families
- Input common-mode range includes ground
- Differential input voltage equal to the power supply voltage

Typical Connection



Connection Diagram



Programming Equation

$$I_{SET} = \frac{(V^+) - (V^-) - 1.3V}{R_{SET}}$$

$$I_{SUPPLY} \approx 22 \times I_{SET}$$

National Semiconductor

November 1982

MA1136 12 V_{DC} Automotive/Instrument Clock Module

General Description

The MA1136 is an electronic digital automotive clock module featuring 4-digit high efficiency LED displays. It is designed to offer the user a low cost automotive or instrument clock module with electronic assembly capability. A minimum number of discrete components are needed to form a complete digital clock for 12 V_{DC} instrument panel applications. Additional components are needed to fully protect against automotive transients and battery reversal conditions.

The MA1136 may also be used with switches to produce a full-featured movement for use in DC operated alarm clock, clock radio, and appliance timer applications. Advanced packaging techniques allow minimum overall size and high reliability in finished products.

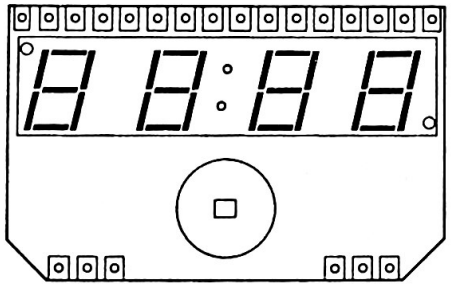
Applications

- In-dash auto clocks
- After-market auto/recreational vehicle clocks
- Aircraft-marine clocks
- 12 V_{DC} operated instruments
- Portable/battery powered instruments

Functional Features

- High intensity
- Available in 0.3" display size with adhesive mylar cover/diffuser and clear surface color
- Low power consumption
- Direct drive LED display/no RFI
- Display brightness control
- Selectable frequency alarm tone output, gated at a 2 Hz rate, provides an easy interface to an 8Ω speaker for alarm clock application
- DC level sleep output provides an easy interface for clock radio and timer applications
- 24-hour output for an optional calendar circuit
- Separate inputs for all settings and display modes
- "One finger" 59-minute sleep counter setting
- Multiple 9-minute snooze control
- 24-hour alarm with ON/OFF control
- PM, colon and alarm ON LED indicators
- Entire display flashes to indicate power loss
- Simple fast/slow setting controls
- Time-set "lockout" feature eliminates accidental time-setting without inhibiting alarm or sleep settings
- Five display modes (time, seconds, alarm, sleep and lamp test)
- Leading zero blanking

Display Outline



Ordering Information

MA1136XZW

- W — CLEAR
- Z — ADHESIVE MYLAR
- X — DISPLAY COLOR
  - R = Red with Black Reflector Face
  - Y = Yellow with Gray Reflector Face
  - G = Green with Green Reflector Face

National Semiconductor

November 1982

MA1142/MA1143 Series Low Cost Digital High Efficiency LED Clock Modules

General Description

The MA1142/MA1143 series of 4-digit LED electronic digital clock modules is designed to offer low cost in a digital clock assembly with a choice of three colors. In addition to a transformer and setting switches, a minimum number of discrete components are required to produce a full-featured movement for use in alarm clock, clock radio, instrument panel clock and appliance timer applications. Advanced packaging techniques guarantee minimum overall size and high reliability in finished products.

Key features include red, green or yellow display; multiple 9-minute snooze; "one finger" sleep setting; easy to use "fast and slow" setting controls; five display modes (time, seconds, alarm, sleep and lamp test); PM, alarm ON and LED colon indicators; power failure indication; time-set lockout; and back-up oscillator for battery powered timekeeping during power loss. All models are designed to generate a selectable frequency alarm tone output gated at a 2 Hz rate (provided the user adds an external resistor and capacitor). Worldwide market flexibility is provided by user-programmable 12 or 24-hour display format, 50 Hz or 60 Hz input frequency selection and fixed or blinking colon indicator. The display brightness level can be varied with a single external potentiometer for continuous control.

Features

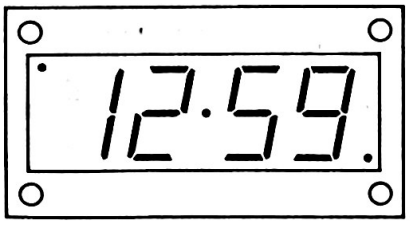
- Red, green or yellow LED display
- Available in two display sizes, 0.7" or 0.5", with or without clear or red lens filter
- "One finger" 59-minute sleep counter setting
- Multiple 9-minute snooze control
- 24-hour alarm with ON/OFF control
- PM, colon and alarm ON LED indicators
- Entire display flashes to indicate power loss
- Simple fast/slow setting controls
- Time set lockout feature eliminates accidental time-setting without inhibiting alarm or sleep settings
- Five display modes (time, seconds, alarm, sleep and lamp test)
- User selectable 12/24-hour, 50 Hz/60 Hz and fixed or flashing colon operation
- Leading zero blanking
- On board zener protection of LEDs
- Direct drive LED display/produces no RFI
- Display brightness control
- Back-up oscillator allows continuous timekeeping during power-line failure with an external 9V battery and 5 MΩ potentiometer

Applications

- Clock radio timers
- Alarm clocks
- Desk clocks
- TV, stereo timers
- Appliance timers
- Instrument panel clocks

Display Outline

MA1142/MA1143



Ordering Information

M A 1 1 4 X X X X

DISPLAY SIZE
2 = 0.5"
3 = 0.7"

LENS SURFACE COLOR
R = Red
W = Clear

SURFACE TYPE
Z = Adhesive Mylar
L = Plastic Lens Cover with Diffuser

DISPLAY COLOR
Y = Yellow
G = Green
R = Red

Circle DATA UPDATE No. 108677

National Semiconductor

November 1982

MCA600ECL/MCA1200ECL ECL 10,000 Macrocell Arrays

General Description

There are two macrocell array (MCA) products available that are compatible with the ECL 10,000 logic family, utilizing the OXISS II process. They have part numbers of MCA1200ECL and MCA600ECL. The MCA1200ECL has approximately 1192 equivalent gates, while the MCA600ECL has approximately 652 equivalent gates when full adders and latches are used in all the cells.

The MCA1200 ECL chip consists of a total of 106 cells. There are 48 major cells (M) or 96 half cells (H), 32 interface cells (I), and 26 output cells (O). The MCA600ECL chip contains 24 major cells (M) or 48 half cells (H), 25 interface cells (I), and 18 output cells (O). Each cell contains a fixed array of unconnected transistors and resistors, and all macrocell array chips are built from a standard semiconductor diffusion set. That is, all chips are identical, and can be prefabricated up to metallization step. The Macrocell Design Library contains more than 100 logic functions called macros. A macro (sometimes called macrocell) is a first layer metal interconnection pattern that interconnects the components (transistors and resistors) of a cell into a specific logic function. The CAD system contains the required first layer metallization pattern for each macro as well as the I/O ports.

The macrocell array is voltage compensated for a 10% tolerance of V_{EE}. Thus, a system designed with the macrocell array can operate with a V_{EE} of $-4.68V$ resulting in approximately 10% less power at the same performance.

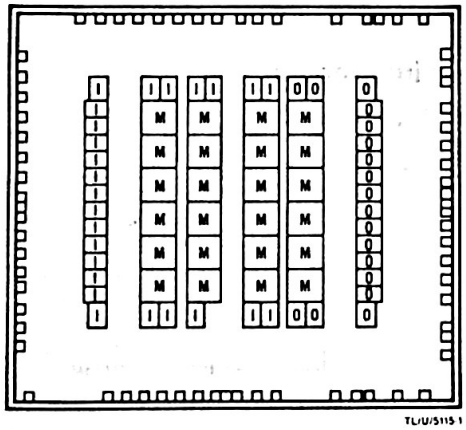
The maximum operating junction temperature is specified at 130°C with the package capable of dissipating 5W of power. A recommended heat sink and 1000 lfpm of air flow result in a thermal resistance, Θ_{JA}, of only 10°C/W for MCA1200 in a 68-pin leadless package. The ambient temperature range is 0°C to 70°C.

The MCA600ECL requires only 500 lfpm of air flow with no heat sink. This results in a typical Θ_{JA} of 22°C/W for all three package types (28-pin, 40-pin, and 68-pin packages).

Features

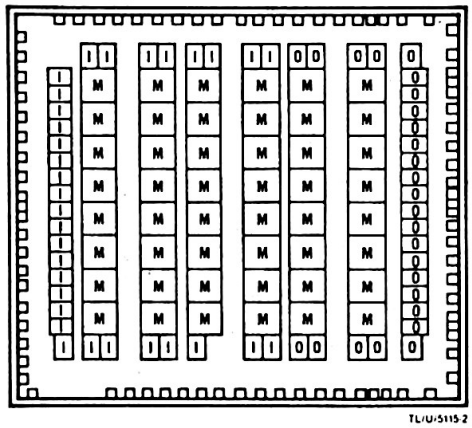
- 106 total cells for MCA1200, 67 total cells for MCA600
- Up to 1192 equivalent gates if full adders and latches are used in all the cells for MCA1200, 652 gates for MCA600
- Up to 904 equivalent gates if flip-flops and latches are used in all the cells for MCA1200, 508 gates for MCA600
- Die size—221 × 252 mils for MCA1200, 174 × 185 mils for MCA600
- Power dissipation—4.0W typical for MCA1200, 2.2W typical for MCA600
- 4.4 mW per equivalent gate (for 904 gates and 4.0W)
- Interface cell delay—0.7 ns to 1.3 ns typ (1.05 ns to 1.7 ns max)
- Major cell delay—0.7 ns to 1.8 ns typ (1.05 ns to 2.35 ns max)
- Output cell delay—1.5 ns to 2.5 ns typ (2.8 ns to 3.8 ns max)
- 8 output cells can drive a 25Ω load
- All output cells can drive 50Ω loads
- Edge speed—1.5 ns typ, 20% to 80% (1.0 ns min)
- Ambient temperature range = 0°C to 70°C (with heat sink and 1000 lfpm air flow for MCA1200, 500 lfpm from MCA600)
- Θ_{JA} = 10°C/W with heat sink and 1000 lfpm air flow for MCA1200 in a 68-pin leadless package
- Maximum operating junction temperature, T_J = 130°C
- Voltage compensated, $V_{EE} = -5.2V \pm 10\%$
- Interfaces with ECL 10k

MCA600ECL



TL/U/5115-1

MCA1200ECL



TL/U/5115-2

National Semiconductor

January 1983

MM52632 32,768-Bit (4096 x 8) MAXI-ROM®

General Description

The MM52632 is a static MOS 32,768-bit read-only memory organized in a 4096-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

Two programmable output-enable controls provide for memory expansion.

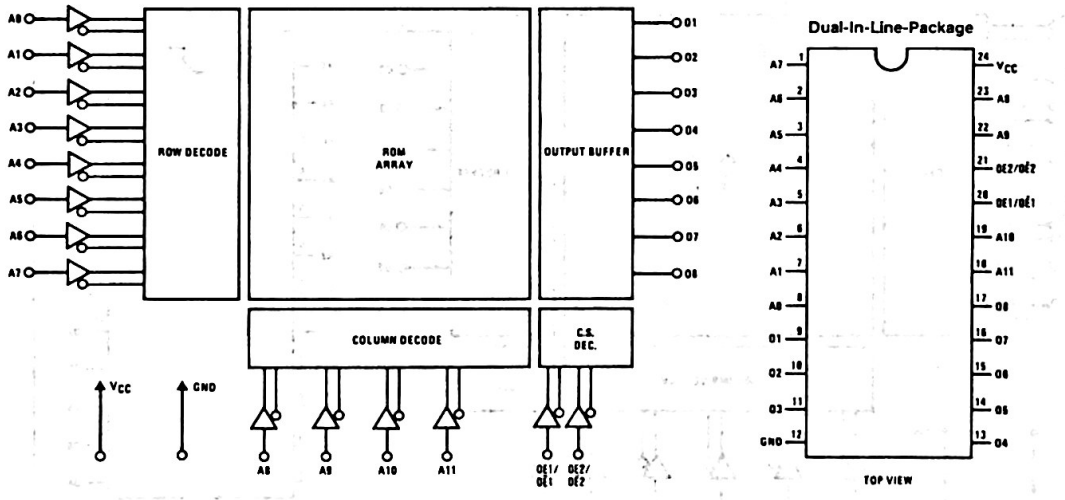
Features

- Fully decoded
- Single 5V power supply
- Inputs and outputs TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Static operation
- TRI-STATE® outputs for bus interface
- Programmable output enables
- 4096-word-by-8-bit organization
- Maximum access time 450 ns
- Industry standard pin outs

Applications

- Microprocessor instruction store
- Control logic
- Table look-up

Block and Connection Diagrams



TL/B/5157-1

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Circle DATA UPDATE No. 110670

National Semiconductor

January 1983

MM52664 65,536-Bit (8192 x 8) MAXI-ROM®

General Description

The MM52664 is a static MOS 65,536-bit read-only memory organized in an 8192-word by 8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

One programmable output-enable control provides for memory expansion.

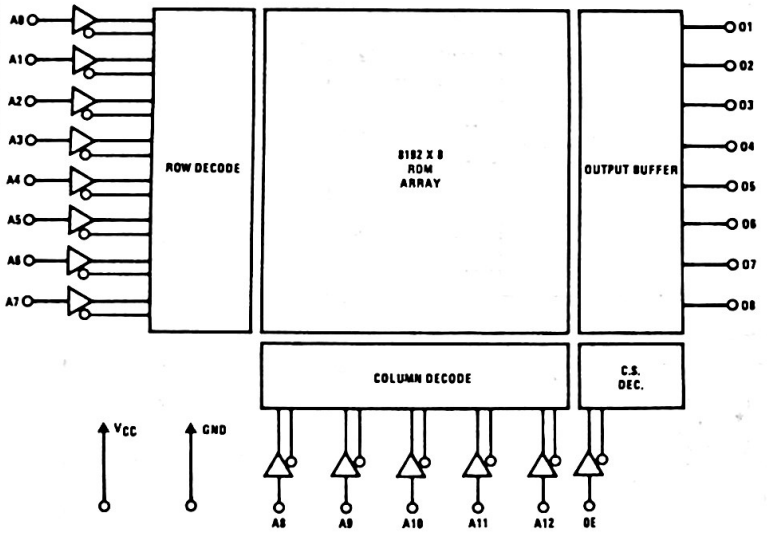
Features

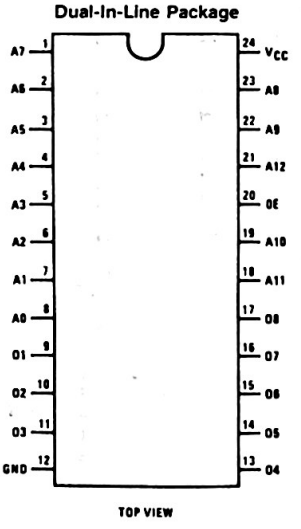
- Fully decoded
- Single 5V power supply
- Inputs and outputs TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Static operation
- TRI-STATE® outputs for bus interface
- Programmable output-enable
- 8192-word-by-8-bit organization
- Maximum access time — 450 ns
- Industry standard pin outs

Applications

- Microprocessor instruction store
- Control logic
- Table look-up

Block and Connection Diagrams





TLB5158-1

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Circle DATA UPDATE No. 110690

National Semiconductor

PRELIMINARY
November 1982

MM54HC10/MM74HC10 Triple 3-Input NAND Gate

General Description

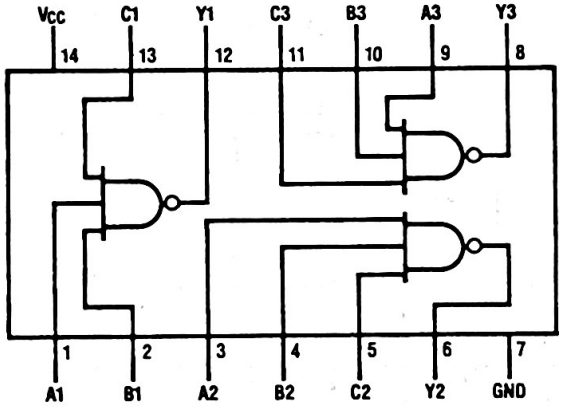
These logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high high noise immunity and the ability to drive 10 LSTTL loads (8 LSTTL loads for 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8ns
- Wide power supply range: 2–6V
- Low quiescent current: 20μA maximum (74HC series)
- Low input current: 1μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

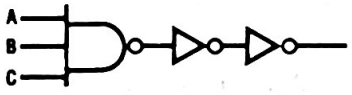
Dual-In-Line Package



$Y = \overline{ABC}$

TL/F/5153-1

Logic Diagram



TL/F/5153-2

National Semiconductor

October 1982

MM54HC14/MM74HC14 Hex Inverting Schmitt Trigger

General Description

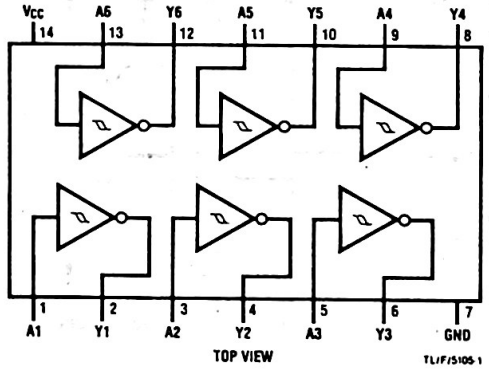
The MM54HC14/MM74HC14 is fabricated with high speed silicon gate CMOS technology. It has the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL (8 LS-TTL loads for 54HC). The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads (74HC series)
- Typical hysteresis voltage: 0.9V

Connection Diagram

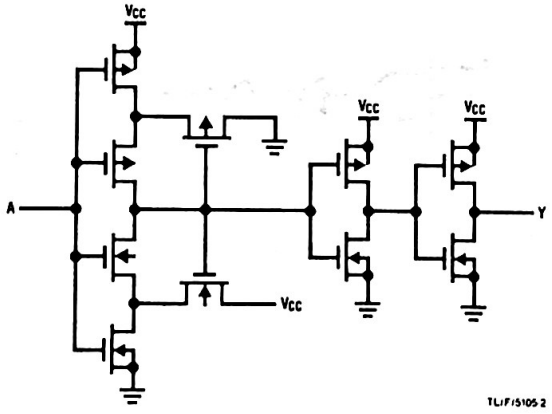
Dual-In-Line Package



TOP VIEW

TL/F/5105-1

Schematic Diagram



TL/F/5105-2

ADVANCED SCHOTTKY DATABOOK

DESCRIPTION

The DM54/74AS family of devices are designed to meet the needs of system designers who require the ultimate in speed. AS achieves the fastest prop delays bipolar technology can offer (2 ns per gate). The AS family also offers significant reduction in power dissipation (8 mW per gate) over present Schottky (54/74S) with toggle rate capability of up to 200 MHz.

The AS family is TTL pinout compatible and offers Schottky (54/74S) drive capability with better fan out, higher noise immunity and faster operation.

For maximum design flexibility and elimination of special drawings, the AS family will be introduced with ±10% VCC over the military and commercial full temp range as standard product. Furthermore, all switching characteristics are guaranteed over the full temperature and V_{CC} range.

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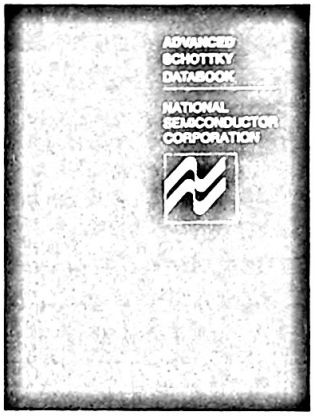

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The Reliability Handbook Volume I penetrates the barrier of technical jargon and procedural ritual that has grown around the subject of semiconductor reliability, enabling the reader to arrive at a clearer understanding in the areas that bear direct concern in the application of semiconductors within the Military/Aerospace electronic systems.

This handbook focuses on areas of concern to all users of semiconductors where device reliability is of paramount importance. It examines the devices themselves and discusses the most widely accepted and specific test procedures designed to test reliability. Throughout, the relationship of electrical, mechanical, environmental and visual tests and inspections to the nature of the device is emphasized. Discussions include the MIL STD-883, MIL-M-38510, VLSI/VHSIC, 883B/RETS™, and 883S/RETS™.

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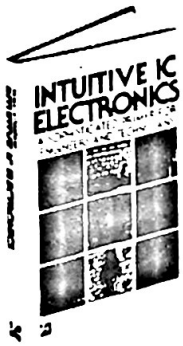

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110670	110690	111535	111538	111542	111543	111560	111563	111570	111580
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PRELIMINARY
December 1982

MM54HC32/MM74HC32 Quad 2-Input OR Gate

General Description

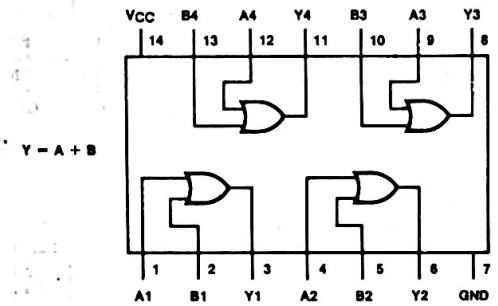
These OR gates utilize silicon gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

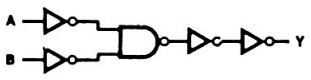
- Typical propagation delay: 10ns
- Wide power supply range: 2-6V
- Low quiescent current: 20μA maximum (74HC series)
- Low input current: 1μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

Dual-In-Line Package



Logic Diagram



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PRELIMINARY
October 1982

MM54HC73/MM74HC73
MM54HC107/MM74HC107
Dual J-K Flip-Flops with Clear

General Description

These high speed J-K Flip-Flops are fabricated with silicon gate CMOS technology. They possess the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads (8 LS-TTL loads for 54HC).

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a low level on the input.

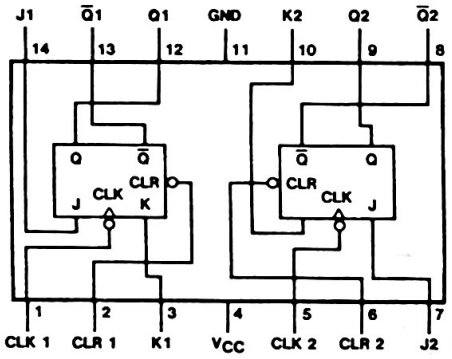
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

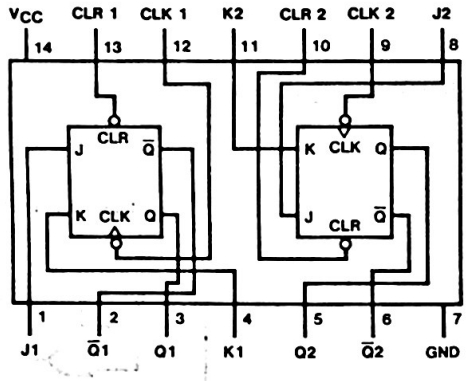
- Typical propagation delay: 16ns
- Wide operating voltage range: 2-6V
- Low input current: 1μA maximum
- Low quiescent current: 40μA (74 series)
- High output drive: 10 LS-TTL loads (74 series)

Connection Diagrams

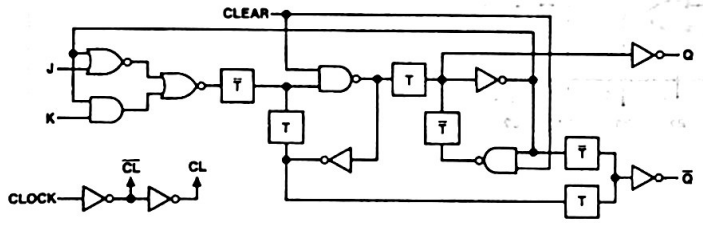
MM54HC73/MM74HC73
Dual-In-Line Package

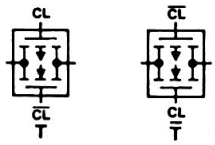


MM54HC107/MM74HC107
Dual-In-Line Package



Logic Diagram





Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

Circle DATA UPDATE No. 111542

National Semiconductor

PRELIMINARY
October 1982

MM54HC74/MM74HC74
Dual D Flip-Flop with Preset and Clear

General Description

The MM54HC74/MM74HC74 utilizes silicon gate CMOS technology to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC).

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

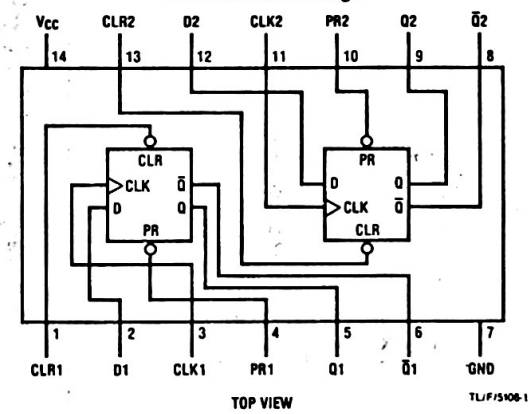
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 40 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5106-1

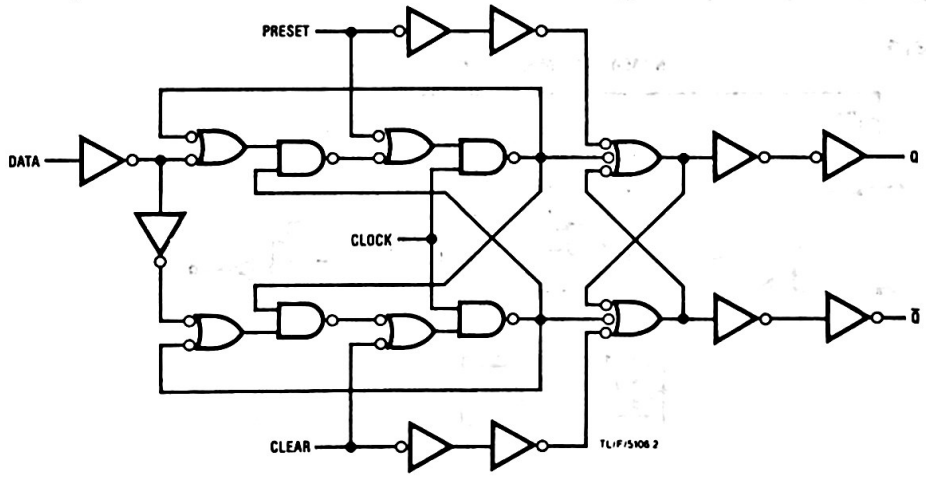
Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Logic Diagram



TL/F/5106-2

National Semiconductor

PRELIMINARY
October 1982

MM54HC113/MM74HC113 Dual J-K Flip-Flops with Preset

General Description

These high speed J-K Flip-Flops are fabricated with silicon gate CMOS technology. They possess the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads (8 LS-TTL loads for 54HC).

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and PRESET inputs and Q and $\overline{Q}$ outputs. PRESET is independent of the clock and accomplished by a low level on the input.

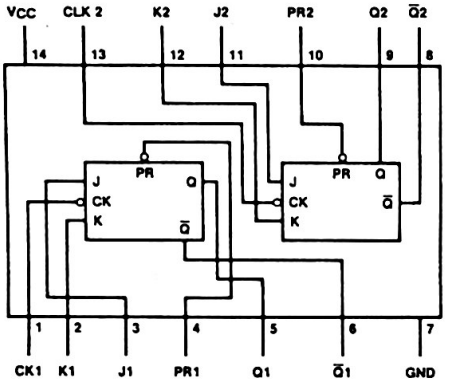
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16nS
- Wide operating voltage range: 2-6V
- Low input current: 1μA maximum
- Low quiescent current: 40μA (74 series)
- High output drive: 10 LS-TTL loads (74 series)

Connection Diagram and Truth Table

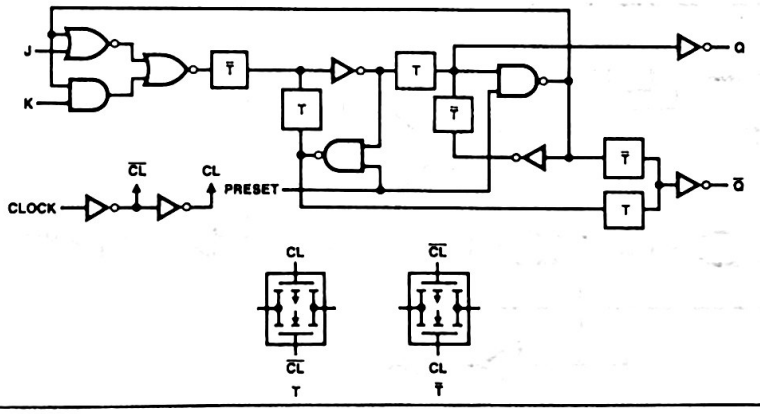
MM54HC113/MM74HC113
Dual-In-Line Package



Inputs				Outputs	
PR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

Logic Diagram

MM54C113/MM74C113



Circle DATA UPDATE No. 111560

National Semiconductor

PRELIMINARY
November 1982

MM54HC138/MM74HC138 3-to-8 Line Decoder

General Description

These devices are high speed silicon gate CMOS decoders, and are well suited to memory address decoding or data routing applications. Both circuits feature high noise immunity and low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

The MM54HC138/MM74HC138 have 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, G2A and G2B) are provided to ease the cascading of decoders.

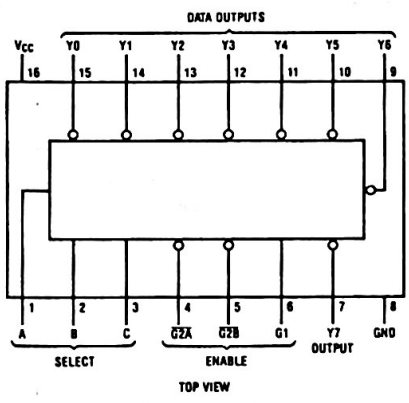
The decoder's outputs can drive 10 low power Schottky TTL equivalent loads (8 loads for 54HC), and are functionally and pin equivalent to the 54LS138/76LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

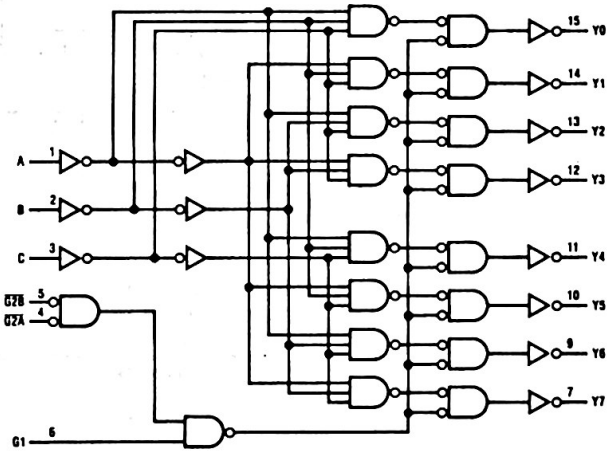
- Typical propagation delay: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

Dual-In-Line Package



Logic Diagram



Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2} = \overline{G2A} + \overline{G2B}$

H = high level, L = low level, X = don't care

National Semiconductor

PRELIMINARY
November 1982

MM54HC153/MM74HC153 Dual 4-Input Multiplexer

General Description

This 4-to-1 line multiplexer is manufactured with high speed silicon gate CMOS technology. It has the low power consumption and high noise immunity of standard CMOS integrated circuits. This device is fully buffered, allowing it to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC). Information on the data inputs of each multiplexer is selected by the address on the A and B inputs, and is presented on the Y outputs. Each multiplexer possesses a strobe input which enables it when taken to a low logic level. When a high logic level is applied to a strobe input, the output of its associated multiplexer is taken low.

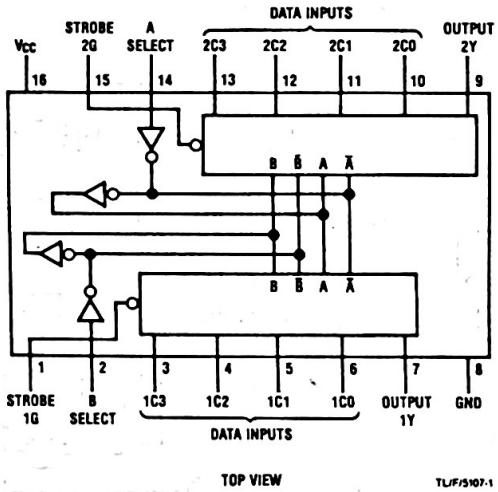
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharged by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5107-1

Truth Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = don't care.

National Semiconductor

PRELIMINARY
November 1982

MM54HC160/MM74HC160
Synchronous Decade Counter with Asynchronous Clear
MM54HC161/MM74HC161
Synchronous Binary Counter with Asynchronous Clear
MM54HC162/MM74HC162
Synchronous Decade Counter with Synchronous Clear
MM54HC163/MM74HC163
Synchronous Binary Counter with Synchronous Clear

General Description

The MM54HC160/MM74HC160, MM54HC161/MM74HC161, MM54HC162/MM74HC162, and MM54HC163/MM74HC163 synchronous presettable counters utilize silicon gate technology and internal look-ahead carry logic for use in high speed counting applications. They offer the high noise immunity and low power consumption inherent to CMOS with speeds similar to low power Schottky TTL. The 'HC160 and the 'HC162 are 4 bit decade counters, and the 'HC161 and the 'HC163 are 4 bit binary counters. All flip-flops are clocked simultaneously on the low to high to transition (positive edge) of the CLOCK input waveform.

These counters may be preset using the LOAD input. Presetting of all four flip-flops is synchronous to the rising edge of CLOCK. When LOAD is held low counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of CLOCK. If the load input is taken high before the positive edge of CLOCK the count operation will be unaffected.

All of these counters may be cleared by utilizing the CLEAR input. The clear function on the MM54HC162/MM74HC162 and MM54HC163/MM74HC163 counters are synchronous to the clock. That is, the counters are cleared on the positive edge of CLOCK while the clear input is held low.

The MM54HC160/MM74HC160 and MM54HC161/MM74HC161 counters are cleared asynchronously. When the CLEAR is taken low the counter is cleared immediately regardless of the CLOCK.

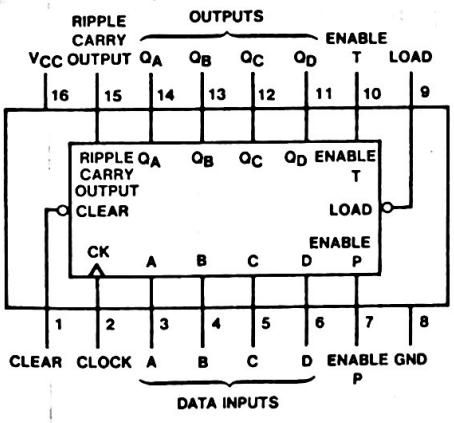
Two active high enable inputs (ENP and ENT) and a RIPPLE CARRY (RC) output are provided to enable easy cascading of counters. Both ENABLE inputs must be high to count. The ENT input also enables the RC output. When enabled, the RC outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of the Q_A output. The RC output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 40MHz
- Typical propagation delay; clock to Q: 18ns
- Low quiescent current: 80μA maximum (74HC series)
- Low input current: 1μA maximum
- Wide power supply range: 2-6V

Connection Diagram



Truth Tables

'HC160/HC161

CLK	CLR	ENP	ENT	Load	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

H = high level, L = low level
X = don't care, ↑ = low to high transition

'HC162/HC163

CLK	CLR	ENP	ENT	Load	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

National Semiconductor

PRELIMINARY
October 1982

MM54HC192/MM74HC192 Synchronous Decade Up/Down Counters MM54HC193/MM74HC193 Synchronous Binary Up/Down Counters

MM54HC192/MM74HC192 Synchronous Decade Up/Down Counters
MM54HC193/MM74HC193 Synchronous Binary Up/Down Counters

General Description

These high speed synchronous counters are fabricated utilizing silicon gate CMOS technology. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HC192/MM74HC192 is a decade counter, and the MM54HC193/MM74HC193 is a binary counter. Both counters have two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

These counters may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

In addition both counters can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counters can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

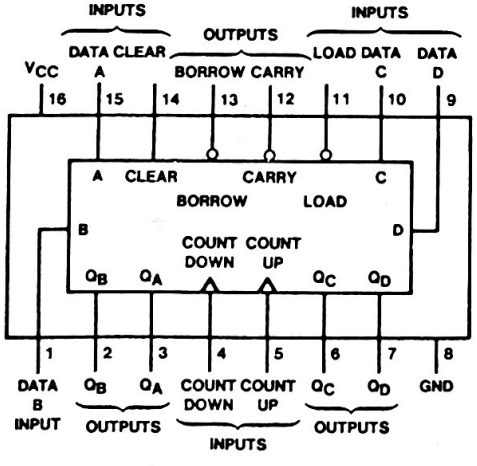
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, Clock to output: 20ns
- Typical operating frequency: 27MHz
- Wide power supply range: 2-6V
- Low quiescent supply current: 80μA maximum (74HC series)
- Low input current: 1μA maximum

Connection Diagram

MM54HC192/MM74HC192
MM54HC193/MM74HC193
Dual-In-Line Package



Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = High level
L = Low level
X = Don't care
↑ = Transition from low-to-high

Circle DATA UPDATE No. 111616

National Semiconductor

PRELIMINARY
November 1982

MM54HC253/MM74HC253
Dual 4-Channel TRI-STATE® Multiplexer

General Description

The MM54HC253/MM74HC253 is fabricated with high speed silicon gate CMOS technology. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the capability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC). The large output drive and TRI-STATE features of this device make it ideally suited for interfacing with bus lines in bus organized systems. When the output control input is taken high, the multiplexer outputs are sent into a high impedance state.

When the output control is held low, the associated multiplexer chooses the correct output channel for the given input signals determined by the select A and B inputs.

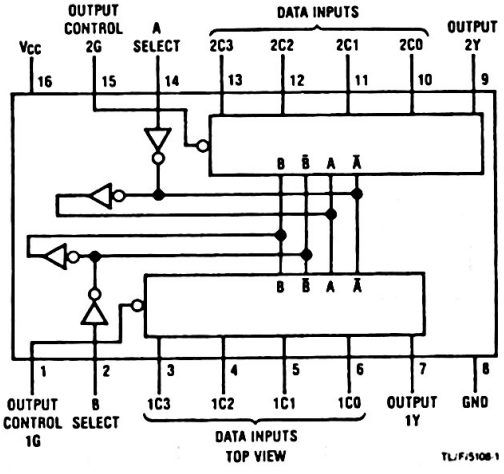
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

Dual-In-Line Package



Truth Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select Inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off).

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Circle DATA UPDATE No. 111621

National Semiconductor

PRELIMINARY
November 1982

MM54HC280/MM74HC280
9-Bit Odd/Even Parity Generator/Checker

General Description

The MM54HC280/MM74HC280 is fabricated with high speed silicon gate CMOS technology. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC).

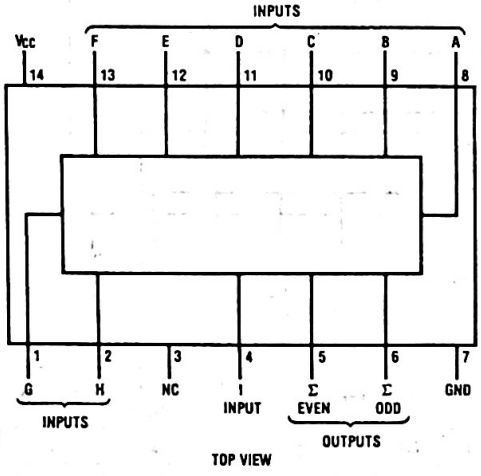
This parity generator/checker features odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading devices. The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 28 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads (74HC)

Connection Diagram

Dual-In-Line Package



TOP VIEW

Function Table

Number of Inputs A thru I that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

National Semiconductor

PRELIMINARY
October 1982

MM54HC374/MM74HC374 TRI-STATE® Octal D-Type Flip-Flop MM54HC534/MM74HC534 TRI-STATE Octal D-Type Flip-Flop with Inverted Outputs

MM54HC374/MM74HC374 TRI-STATE Octal D-Type Flip-Flop
MM54HC534/MM74HC534 TRI-STATE Octal D-Type Flip-Flop with Inverted Outputs

General Description

These high speed Octal D-Type Flip-Flops are manufactured with silicon gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads (12 LS-TTL loads for 54HC). Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

The MM54HC374/MM74HC374 and MM54HC534/MM74HC534 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q(374) or $\overline{Q}$(534) outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

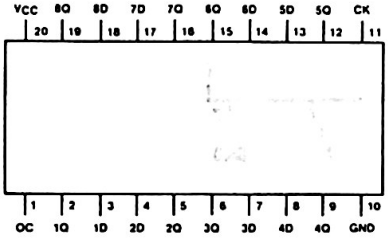
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

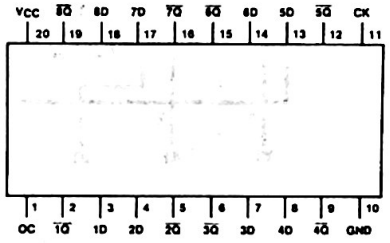
- Typical propagation delay: 15ns
- Wide operating voltage range: 2-6V
- Low input current: 1μA maximum
- Low quiescent current: 80μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads (74HC series), 12 LS-TTL loads (54HC series)

Connection Diagrams

MM54HC374/MM74HC374
Dual-In-Line Package



MM54HC534/MM74HC534
Dual-In-Line Package



Truth Table

Output Control	Clock	Data	Output (374)	Output (534)
L	↑	H	H	L
L	↑	L	L	H
L	L	X	Q_0	$\overline{Q}_0$
H	X	X	Z	Z

H = High Level, L = Low Level,
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established

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Circle DATA UPDATE No. 111580

National Semiconductor

PRELIMINARY
November 1982

MM54HC4002/MM74HC4002 Dual 4-Input NOR Gate

General Description

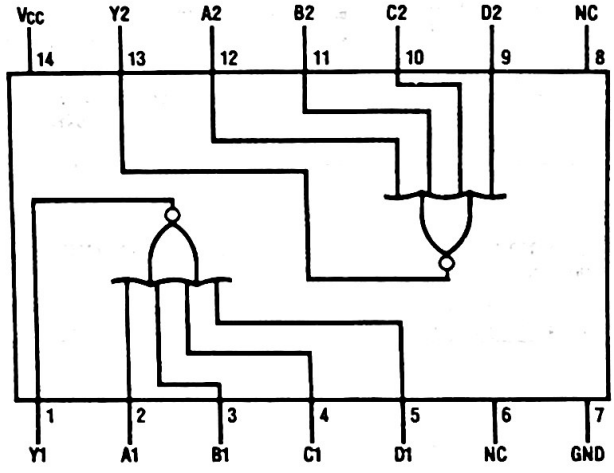
These NOR gates utilize silicon gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. The 54HC4002/74HC4002 is functionally equivalent and pin-out compatible with the CD4002B. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 11ns
- Wide power supply range: 2–6V
- Low quiescent current: 20μA maximum (74HC series)
- Low input current: 1μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5154-1

$$Y = \overline{A + B + C + D}$$

Circle DATA UPDATE No. 111649

National Semiconductor

PRELIMINARY
November 1982

MM54HC4075/MM74HC4075 Triple 3-Input OR Gate

General Description

These OR gates utilize silicon gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads (8 LS-TTL loads for 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. The 54HC4075/74HC4075 is functionally equivalent and pin-out compatible with the CD4075B and MC14075B metal gate CMOS devices. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

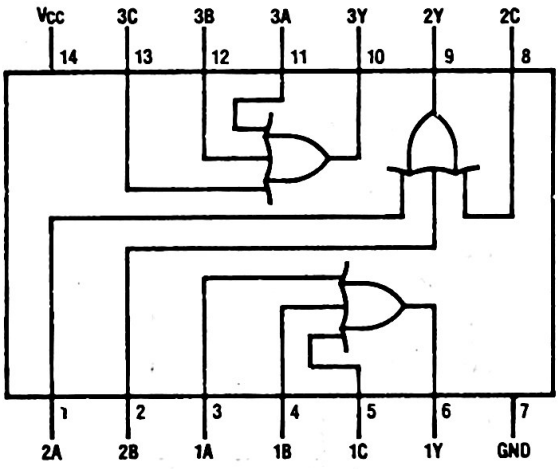
Features

- Typical propagation delay: 11ns
- Wide power supply range: 2–6V
- Low quiescent current: 20μA maximum (74HC series)
- Low input current: 1μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

Dual-In-Line Package

$Y = A + B + C$



TL/F/5155-1

Circle DATA UPDATE No. 111653

National Semiconductor

PRELIMINARY
December 1982

MM54HC4078/MM74HC4078 8-Input NOR/OR Gate

General Description

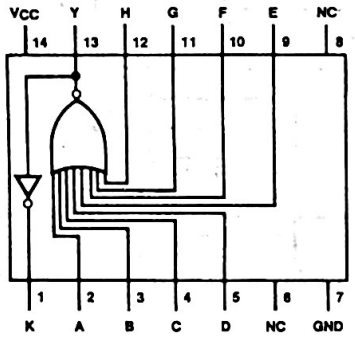
These NOR gates utilize silicon gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. Both outputs are buffered, providing high noise immunity and the ability to drive 10 LS-TTL loads (8 LS-TTL loads for the 54HC). The 54HC4078/74HC4078 is functionally equivalent and pin-out compatible with the CD4078B. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15ns
- Wide power supply range: 2-6V
- Low quiescent current: 20μA maximum (74HC series)
- Low input current: 1μA maximum
- Fanout of 10 LS-TTL loads (74HC Series)

Connection Diagram

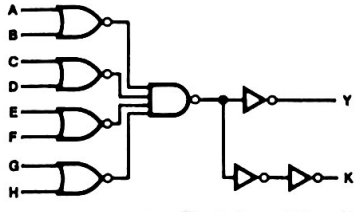
Dual-In-Line Package



$Y = \overline{A + B + C + D + E + F + G + H}$

$K = \overline{Y}$

Logic Diagram



Circle DATA UPDATE No. 111652

National Semiconductor

PRELIMINARY
November 1982

MM74C945, MM74C947 4-Digit Up/Down Counter/Latch/Decoder Driver

General Description

The MM74C945, MM74C947 are 4-digit counters for directly driving LCD displays. The MM74C945 contains a 4-decade up/down counter, output latches, counter/latch select multiplexer and 7-segment decoders. Also included are the backplane oscillator/driver, segment drivers and display blanking circuitry.

The MM74C947 differs from the MM74C945 in that it has no counter/latch multiplexer, but provides true leading zero blanking. All leading zeroes are automatically blanked except the least significant digit, which can be optionally blanked.

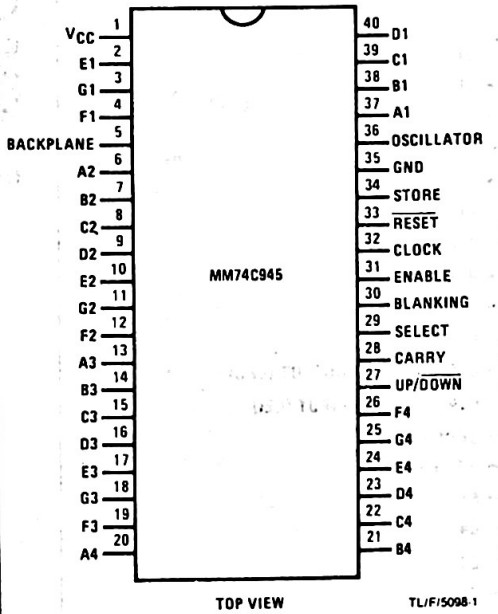
Both devices provide 28-segment outputs to drive a 4-digit display. Segment and backplane waveforms are generated internally, but can also be slaved to an external signal. This facilitates cascading of multiple displays.

Features

- 4-decade up/down count
- Direct 4-digit drive for high contrast and long display life
- Carry/borrow out for cascading counters
- Schmitt trigger clock input
- MM74C945 has display select to allow viewing of counter or latch
- Store and reset inputs allow operation as frequency or period counter
- MM74C947 has true ripple blanking; least significant digit may be optionally blanked

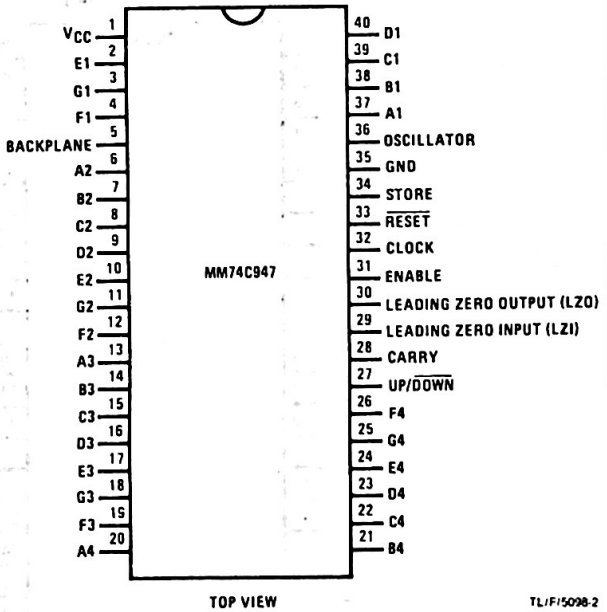
Connection Diagrams

Dual-In-Line Package



TOP VIEW TL/F/5098-1

Dual-In-Line Package



TOP VIEW TL/F/5098-2

National Semiconductor

PRELIMINARY
November 1982

MM74C946 4½-Digit Counter/Decoder/ Driver for LCD Displays

General Description

The MM74C946 is a 4½-digit CMOS counter which contains a counter chain, decoders, output latches, LCD segment drivers, count inhibit and backplane oscillator/driver circuitry. This device also contains leading zero blanking and a carry output to increase flexibility and facilitate cascading of multiple 4-digit sections.

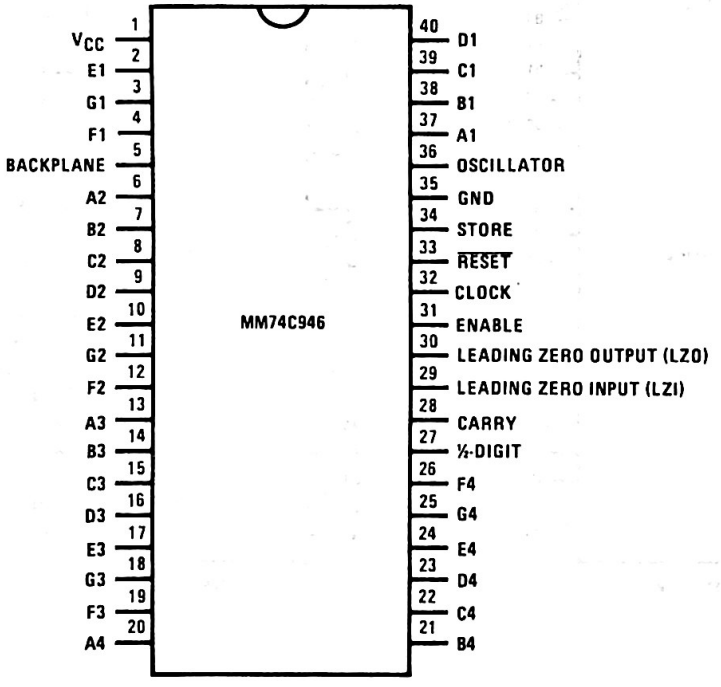
This device provides 29 segment outputs to drive a standard 4½-digit liquid crystal display. An on-chip backplane oscillator/driver is also provided. This can be disabled by grounding the oscillator pin, thus allowing the device to be slaved to an external backplane signal via the backplane pin.

Features

- Low power operation—less than 100 μW quiescent
- Direct 4½-digit 7-segment display drive for higher contrast and long display life
- Pin compatible to Intersil's ICM7224
- Store and $\overline{\text{Reset}}$ inputs permit operation as frequency or period counter
- True count inhibit disables first counter stage
- Carry output for cascading 4-digit blocks
- Schmitt trigger on the clock input allows operation in noisy environments or with slowly changing inputs
- Leading zero blanking input and output for correct leading zero blanking with cascaded devices
- On-chip backplane oscillator/driver which can be disabled to permit slaving of multiple devices to an external backplane signal

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5102-1

National Semiconductor

October 1982

National Masked Logic (NML) Family

General Description

National Masked Logic (NML) is an extension of Programmable Array Logic (PAL®) technology which substitutes metal interconnects, fabricated during the manufacturing process, for the field programmable fuse links found on the PAL approach when sufficient quantities per pattern are required. While the exact number of units to justify the masked approach varies over time due to increasing and decreasing component and labor costs, it should remain in the several thousands per pattern.

PAL/NML technology allows the user to replace several SSI/MSI logic devices with a single 20- or 24-pin thin-DIP PAL/NML device. Typical chip count reduction runs from 4:1 to 12:1.

The family lets the systems engineer customize his chip by configuring AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus transferred from PC board to silicon where they can be easily modified during prototype check-out by using PALs and then switching to the NML parts when high volume production is achieved.

The NML transfer function is the familiar sum of products with a single array of program links. Unlike the ROM, the NML is a programmable AND array driving a fixed OR array (the ROM is a fixed AND array driving a programmable OR array). In addition, the NML provides these options:

- Variable input/output pin ratio
- Programmable 3-state outputs
- Registers with feedback

Registers consist of D-type flip-flops which are loaded on the low-to-high transition of the clock. Logic diagrams are shown with all cross points disconnected, enabling the designer use of the diagrams as coding sheets.

The PAL version of this family is programmed on conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to make verification difficult. This feature gives the user a proprietary circuit which is very difficult to copy. Specifications for the PAL and NML devices are identical, which permit substitution of one device for the other with a minimum of difficulty.

Features

- Programmable replacement for conventional TTL logic
- 20-pin DIP packages
- Programmable prototyping tool (PALs)
- Special feature reduces possibility of copying by competitors

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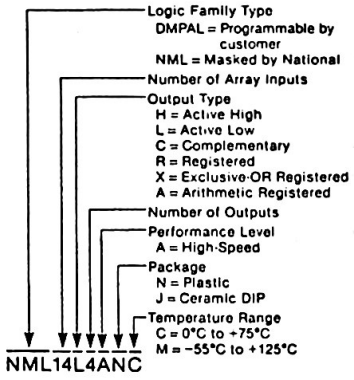
Ordering Information

Part Number System



20-Pin Family

Part Number	Description	
NML10H8	OCTAL	10 Input AND OR Gate Array
NML12H6	HEX	12 Input AND OR Gate Array
NML14H4	QUAD	14 Input AND OR Gate Array
NML16H2	DUAL	16 Input AND OR Gate Array
NML16C1	16 Input	16 Input AND-OR/AND OR-INVERT Gate Array
NML10L8	OCTAL	10 Input AND-OR INVERT Gate Array
NML12L6	HEX	12 Input AND OR-INVERT Gate Array
NML14L4	QUAD	14 Input AND OR INVERT Gate Array
NML16L2	DUAL	16 Input AND-OR-INVERT Gate Array
NML16L8	OCTAL	16 Input AND-OR-INVERT Gate Array
NML16R8	OCTAL	16 Input Registered AND-OR Gate Array
NML16R6	HEX	16 Input Registered AND OR Gate Array
NML16R4	QUAD	16 Input Registered AND-OR Gate Array
NML16X4	QUAD	16 Input Registered AND-OR-XOR Gate Array
NML16A4	QUAD	16 Input Registered AND-CARRY-OR-XOR Gate Array

24-Pin Family

Part Number	Description	
NML12L10	DECA	12 Input AND OR INVERT Gate Array
NML14L8	OCTAL	14 Input AND-OR-INVERT Gate Array
NML16L6	HEX	16 Input AND-OR INVERT Gate Array
NML18L4	QUAD	18 Input AND OR INVERT Gate Array
NML20L2	DUAL	20 Input AND OR-INVERT Gate Array
NML20L1		20 Input AND OR/AND OR-INVERT Gate Array
NML20L10	DECA	20 Input AND OR INVERT Gate Array
NML20X10	DECA	20 Input Registered AND-OR-XOR Gate Array
NML20X8	OCTAL	20 Input Registered AND-OR-XOR Gate Array
NML20X4	QUAD	20 Input Registered AND-OR-XOR Gate Array

Circle DATA UPDATE No. 114350

National Semiconductor

PRELIMINARY
January 1983

NS16008S-6, NS16008S-4 High-Performance 8-Bit Microprocessors

NS16008S-6, NS16008S-4 High-Performance 8-Bit Microprocessors

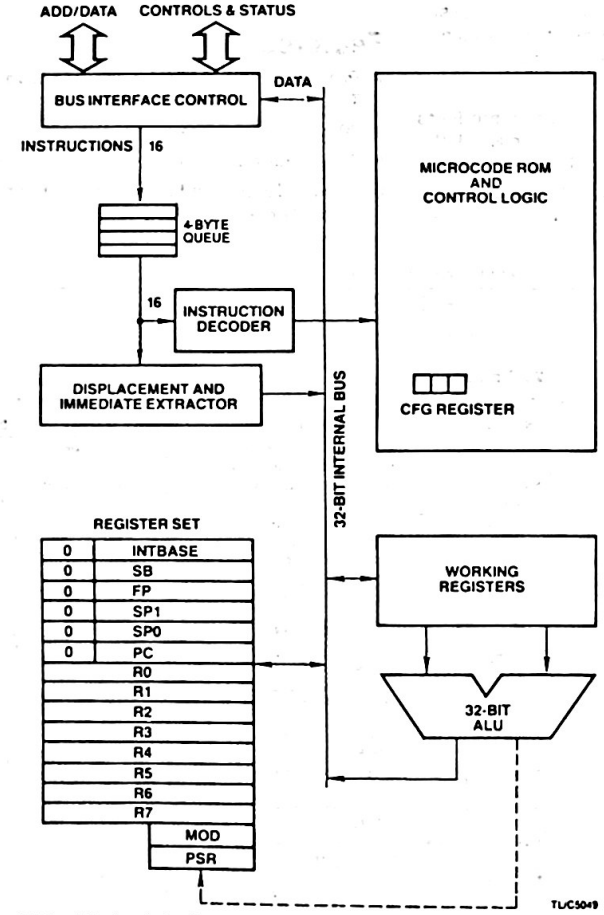
General Description

The NS16008 functions as a Central Processing Unit (CPU) in National Semiconductor's NS16000 microcomputer family. It has been designed to optimally support microprocessor users who need the ability to use a large addressing space for large programs and/or large data structures. Because large programs must realistically be generated and maintained in high-level languages, the NS16000 architecture provides for very efficient compilation while remaining easy to program at the assembler level for optimizations. The NS16008 represents an implementation of this architecture for 8-bit systems. High-performance Floating-Point instructions are provided with the NS16081 Floating-Point Unit (FPU). The NS16008S-4 and NS16008S-6 have different timing parameters. Refer to Section 4 for timing specifications.

Features

- 32-Bit Architecture and Implementation
- 8-bit Bus for Low System Cost
- 16-MByte Uniform Addressing Space
- Powerful Instruction Set
  - — General Two-Address Capability
  - — Very High Degree of Symmetry
  - — Addressing Modes Optimized for High-Level Language References
  - — Expansion via Slave Processors or Traps
- High-Speed XMOS Technology
- Single 5V Supply
- 48-Pin Dual-In-Line Package

NS16008 CPU Block Diagram



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STARPLEX II™ is a trademark of National Semiconductor Corp

 TL/C 5049

Circle DATA UPDATE No. 112348

NS16081 Floating-Point Unit

General Description

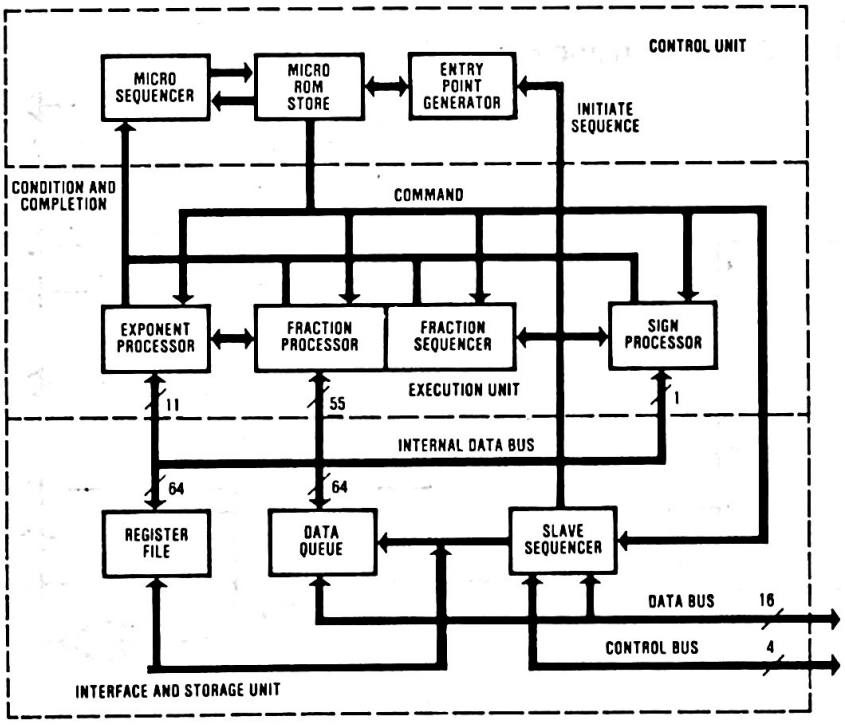
The NS16081 is the Floating-Point Unit (FPU) in the NS16000 microprocessor family. The NS16081 operates as a slave processor, and the NS16081 instruction set appears to the programmer as part of the NS16000 instruction set. Thus, the user can utilize all the powerful addressing modes and data types present in the NS16000 architecture. The FPU performs both single-precision (32-bit) and double-precision (64-bit) floating-point arithmetic, and conforms to the proposed IEEE format. The FPU instruction set includes Add, Subtract, Multiply, Divide, and other popular arithmetic operations. The FPU is compatible with all microprocessors in the NS16000 family.

Features

- Both 32-bit and 64-bit operation
- Eight on-board, general-purpose, 32-bit registers
- Conforms to proposed IEEE format
- Accepts direct memory-to-memory operation
- High-speed execution—typical values (at 10MHz) are:

	32-bit	64-bit
Add	7.4 μs	7.4 μs
Multiply	4.8 μs	6.2 μs
Divide	8.9 μs	11.8 μs

- High-speed XMOS™ technology
- Single, +5V supply
- 24-pin package



FPU Block Diagram

OC1799-1

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Circle DATA UPDATE No. 630490

National Semiconductor

PRELIMINARY
November 1982

NS16201-6 Timing Control Unit

General Description

The NS16201 Timing Control Unit (TCU) is a 24-pin device fabricated on a Schottky bipolar process. It provides the 2 phase MOS clock drivers, system control logic (read, write, and data buffer enable) and cycle extension logic for the NS16000 family.

A crystal or external signal may be used as the 2× frequency source. Besides the 2 phase MPU clock outputs (PHI1 and PHI2), there are two other clock outputs (TTL-compatible) available for system timing use. One of these is a fast clock (FCLK), at twice the MPU clock frequency (i.e, at the crystal frequency). The other is a TTL version of PHI1 (CTTL).

The cycle extension features include:

- Digitally programmable wait state inputs ($\overline{WAITn}$)
- Peripheral (slow) cycle to accommodate slower MOS peripheral interface ICs (where just adding wait states is not adequate)
- Cycle Hold between the first (T1) and second (T2) timing states to allow additional time for arbitration prior to generating control signals.

Features

- 2 phase full V_{CC} swing high capacitance clock drivers
- 4-bit input ($\overline{WAITn}$) allowing precise specification of from 0 to 15 wait states
- Cycle Hold for system arbitration and/or memory refresh
- System timing (CTTL and FCLK) and control ($\overline{RD}$, $\overline{WR}$, and $\overline{DBE}$) outputs
- General purpose Timing State Output ($\overline{TSO}$) that identifies internal states
- Support of slow MOS peripheral interface ICs (e.g., 8080 series)
- Provides "ready" (RDY) output for NS16000 MPUs
- Synchronous system reset generation from Schmitt trigger input
- Single 5V power supply
- 24-pin dual-in-line package

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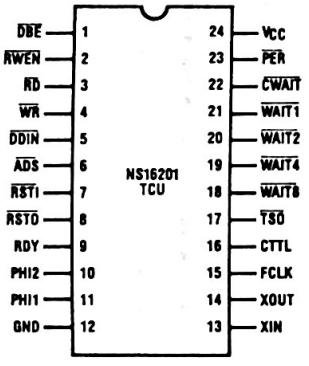
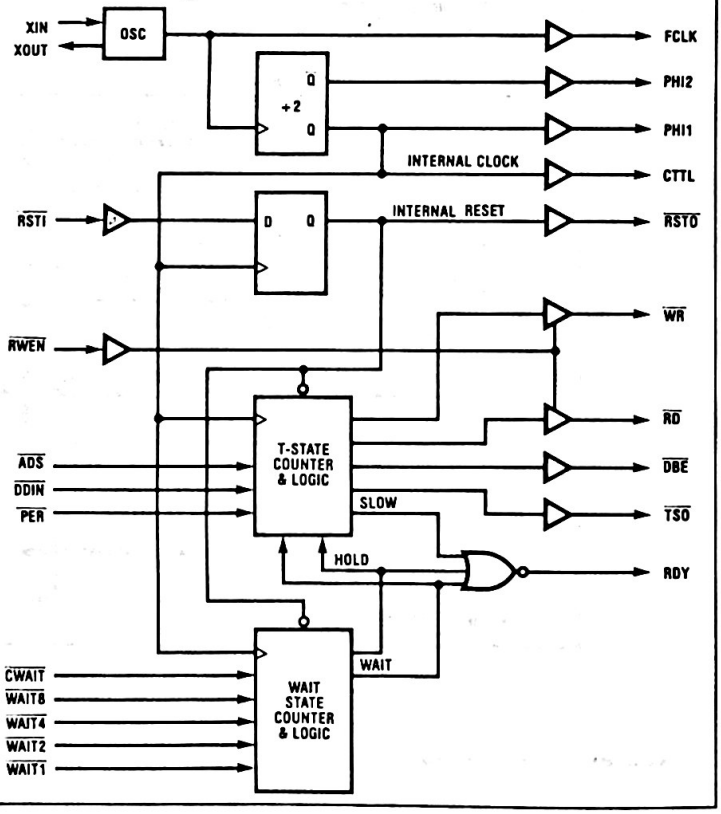
NS16201 TCU Connection and Block Diagrams





Circle DATA UPDATE No. 112360

National Semiconductor

PRELIMINARY
October 1982

NS16202 Interrupt Control Unit

General Description

The NS16202 Interrupt Control Unit (ICU) is the interrupt controller for the NS16000 microprocessor family. It is a support circuit that minimizes the software and real-time overhead required to handle multi-level, prioritized interrupts. A single NS16202 manages up to 16 interrupt sources, resolves interrupt priorities, and supplies a single-byte interrupt vector to the CPU.

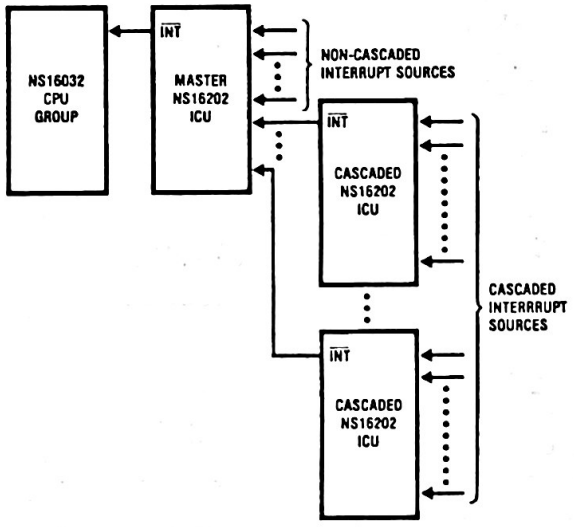
The NS16202 can operate in either of two data bus modes: 8-bit and 16-bit. In the 8-bit mode, up to 16 hardware interrupts with programmable priorities can be handled. In the 16-bit mode, 8 hardware and 8 software interrupts are possible. In either mode, up to 16 additional ICUs may be cascaded to handle a maximum of 256 interrupts.

Two 16-bit counters, which may be concatenated under program control into a single 32-bit counter, are also available for real time applications.

Features

- 16 maskable interrupt sources, cascadable to 256
- Programmable 8- or 16-bit data bus mode
- Edge or level triggering for each hardware interrupt with individually selectable polarities
- 8 software interrupts
- Fixed or rotating priority modes
- Two 16-bit, DC to 10MHz counters, that may be concatenated into a single 32-bit counter
- Optional 8-bit I/O port available in 8-bit data bus mode
- High-speed XMOS technology
- Single, +5V supply
- 40-pin, dual in-line package

NS16202 Basic System Configuration



TL/C/5117-1

National Semiconductor

PRELIMINARY
November 1982

NS16032S-6, NS16032S-4
High-Performance Microprocessors

General Description

The NS16032 functions as a central processing unit (CPU) in National Semiconductor's NS16000 microprocessor family. It has been designed to optimally support microprocessor users who need the ability to use a large addressing space for large programs and/or large data structures. Because large programs must realistically be generated and maintained in high-level languages, the NS16000 architecture provides for very efficient compilation while remaining easy to program at the assembler level for optimizations. NS16000 architecture provides for full virtual memory capability, in conjunction with with the NS16082 Memory Management Unit (MMU). High performance floating-point instructions are provided with the NS16081 Floating-Point Unit (FPU). The NS16032S-4 and NS16032S-6 have different timing parameters. Refer to Section 4 for timing specifications.

Features

- 32-bit Architecture and Implementation
- 16-MByte Uniform Addressing Space
- Powerful Instruction Set
  - — General 2-Address Capability
  - — Very High Degree of Symmetry
  - — Addressing Modes Optimized for High-Level Language References
- High-Speed XMOS Technology
- Single 5V Supply
- 48-pin Dual-In-Line Package

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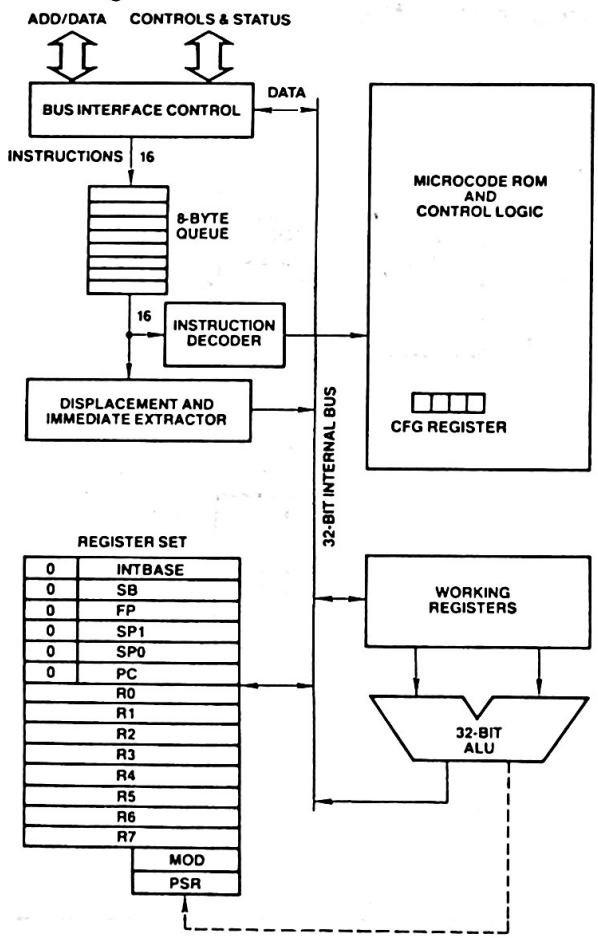
VAX™ is a trademark of Digital Equipment Corp.

NS16032-6 CPU Block Diagram



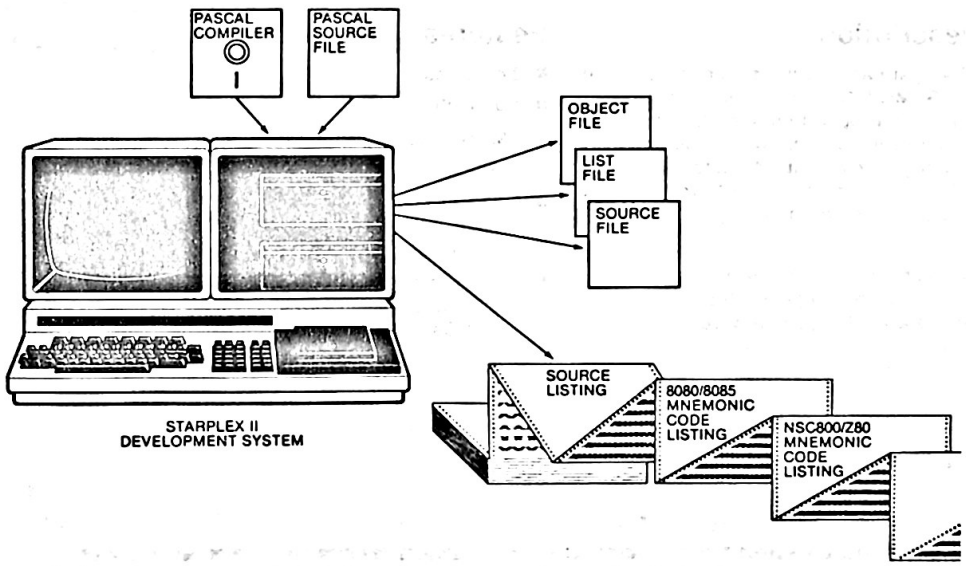
Circle DATA UPDATE No. 112361

National Semiconductor

October 1982

PASCAL

PASCAL High Level Language Compiler For STARPLEX II™ Development Systems



- **Executes On All STARPLEX II Development Systems**
- **Compatible With Existing ISO Standard PASCAL**
- **Highly Portable And Extended Source Programs**
- **Code Generation For 8080/8085 and NSC800™/Z80® Microprocessors**
- **Relocatable And Linkable Object Code Output**
- **Reentrant Procedures as Specified by User**
- **Extensions For Easy Hardware Access Via High Level Statements (Absolute Addresses and Input/Output Ports)**

Product Description

PASCAL is a high level language compiler designed for STARPLEX II Development Systems. Available in two versions, this highly efficient and powerful compiler generates relocatable object code for 8080/8085 and NSC800/Z80 microprocessors.

PASCAL has proven to be one of the most popular, effective and powerful program development tools available today. With STARPLEX II PASCAL, programmer productivity is greatly improved because the programmer can concentrate on system development rather than all the details of assembly languages. Since PASCAL uses data structures that are very close to typical microprocessor architectures, it allows for efficient use of the machine. PASCAL programs are efficiently converted to assembly language instructions thus requiring fewer statements. Software development and maintenance costs are significantly reduced.

Free form PASCAL source programs are efficiently and effectively converted into 8080/8085 and NSC800/Z80 assembly language instructions. A given program, when written in PASCAL, requires much fewer statements than would the equivalent program written in assembly language. Thus, software development and maintenance costs are significantly reduced due to the block oriented structure that results naturally from the use of PASCAL. User programming conventions and structured programming techniques are easily accommodated by the free form source statements of PASCAL.

Circle DATA UPDATE No. 114404

National Semiconductor

PRELIMINARY
December 1982

SCX 6224A High-Performance 2.4k CMOS Gate Array With 2μ Gate Feature Sizes

General Description

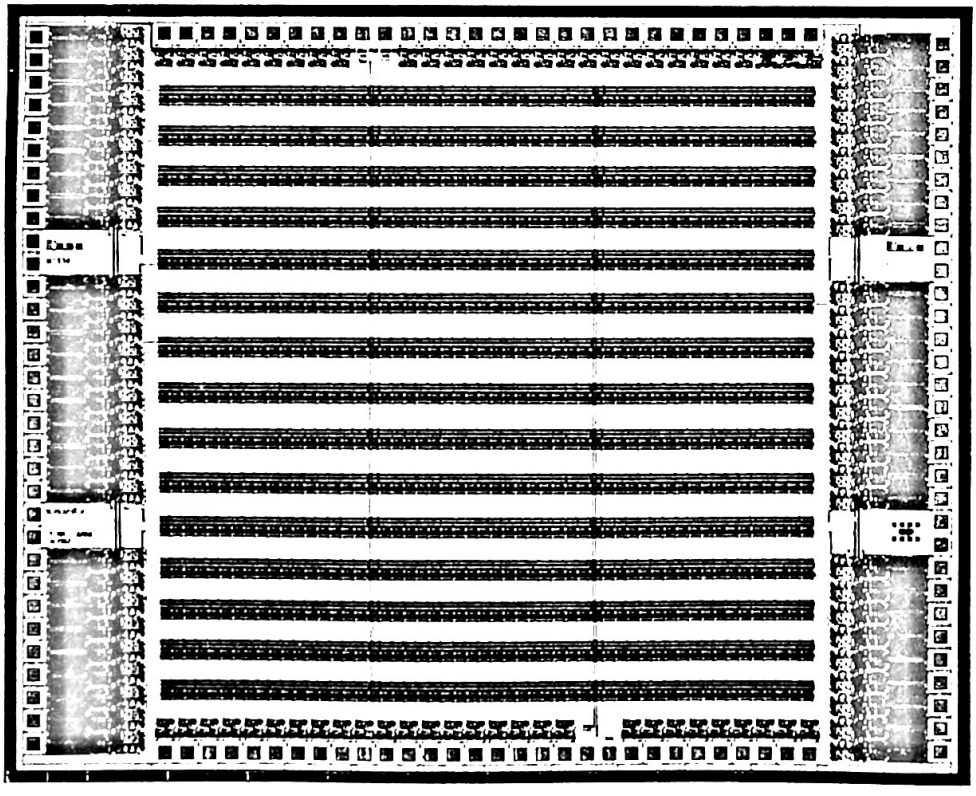
This versatile 2.4k gate array utilizes silicon-gate dual-layer metal CMOS (M^2CMOS) technology with 2μ gate feature sizes to achieve operating speeds better than S-TTL with the inherent lower power consumption of standard CMOS integrated circuits. All outputs have the ability to drive 10 LSTTL loads. All inputs have high noise immunity and are protected from damage due to static discharge.

To enhance user applications, the device is offered in three attractive 124-pin package options. Smaller pin count packages are available upon request.

Features

- 2.4k gates
- 1.0ns internal t_{PD}
- CMOS power dissipation
- "LS" drive capability
- Full design automation support
  - —80% utilization
  - —100% auto place and route
- 124 pins maximum
  - —55 inputs
  - —56 I/Os
  - —6 V_{DD}
  - —6 V_{SS}
  - —1 test

SCX 6224A Topology



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Circle DATA UPDATE No. 113587

SCX 6224A High-Performance 2.4k CMOS Gate Array With 2μ Gate Feature Sizes

National Semiconductor

October 1982

SCX 6324A M²CMOS™ Gate Array NS000U Option User's Note

Introduction

The SCX 6324A CMOS 2.4k Gate Array is fabricated on a 3-micron, dual metal, N- Well, 5V M²CMOS Process which typically provides internal propagation delay of <2ns for a 2-input NAND gate driving an IPF load.

The Test Chip Option of the SCX 6324A (NS000U option) contains all macro cells currently available for design (as of October, 1982). It is intended for engineering evaluation and as a sampling part for AC performance demonstration.

A schematic drawing follows and a test setup scheme is shown on page 5.

Test Set Up

The Test Chip option of the SCX 6324A contains many circuitries for engineering evaluation of macro functions that are currently available. Some circuits may have unprotected inputs/outputs, thus evaluations should be done under a controlled environment. Users are advised to use only those circuits that are mentioned in this note. Connections to any other pins may cause damage to the device.

A test set-up scheme is suggested in Figure 4 for reference, together with a selection table for each macro given in Table 1.

Input Pull-Up: All inputs (except pins 87 and 88) are provided with internal pull-up; grounded inputs will source approximately 8μA each at 25°C and V_{DD} = 5V.

AC Performance of a Macro: The outputs of all macros are fed to the external pins via a MUX and an output buffer, so their exact AC performance should be found by subtracting the delay due to these MUXs and buffers. Pins 59 and 55 (labelled as "Input signal reference") can be used to determine this extra delay.

Internal TRI-STATE® Macro: S9 and S10 are TRI-STATE buffers intended for use within the array. They are brought out to the external pin in this Test Chip option. A scope probe with low loading should be used to give better approximation of their performance. A low capacitance FET probe is recommended. It is unlikely that much less than 8-10pF of parasitic loading can be achieved. (See Note 2.)

Unprotected I/O Pins: There are I/O pins in this option that are not protected. Extreme care should be exercised in using them to avoid latch-up, oxide rupture, etc.

Metal Loading Evaluation: Three strings of inverters are included in this Test Chip for the metal loading evaluation. One is without any extra metal loading except for interconnect; the other two are loaded with 200-mil run of either metal 1 or metal 2 at each inverter stage. Refer to the schematic drawing for details. (See Note 1.)

1. Other than on these gate strings (see "Metal Loading Evaluation" above), no additional loading capacitance is added. All other macros are generally connected with a minimal amount of interconnect—the amount of parasitic strays incurred is not shown.
2. All macros intended for internal array use, but brought directly to output pins, are *not* protected against latch-up. (All true output buffer options of the I/O are fully protected.)

On-Chip Test Circuit

All options of the SCX 6324A are provided with an on-chip test circuitry, at the cost of a single input pin, to create TEST MODE. With this pin active (LOW), two additional pre-defined inputs are jointly employed to force all outputs to HIGH, LOW or HI-Z states and thus reduce test time in gathering output parametrics at sort. These two pins further function as conventional inputs (either TTL or CMOS when in TEST MODE, HIGH) with no performance penalty apparent to the user.

TEST MODE (TMC): A LOW at this input will activate the test circuitry. All output buffers are to be driven by TEST DATA (DT) and TRI-STATE (TEST) pins.

TRI-STATE (TEST): A LOW at this input, together with TMC low, puts all TRI-STATE output buffers to HI-Z state.

TEST DATA (DT): Input to this pin, with TMC low, forces all outputs to either HIGH or LOW.

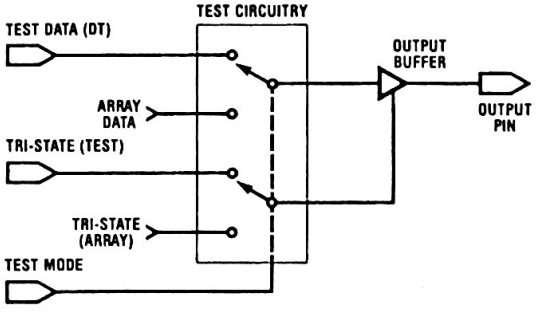

FIGURE 1

TRI-STATE® is a registered trademark of National Semiconductor Corp.
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Page Count: 176 Price: $6.00 Year: 1982

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